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ABSTRACT

Previous research activity at The George Washington University has demonstrated the feasibility of designing a compiler which accepts a high level (programming) language (HLL) and produces microcode for a computer with a horizontal control word format. On going research activity described herein is demonstrating the feasibility of designing a compiler with PASCAL as an input HLL that can generate microcode for the DEC VAX 11/780 computer which is installed in the BMDATC Distributed Data Processing (DDP) Test Bed. The effort described has as its goal the installation of this compiler at the Test Bed and to interface it with the "User Microprogramming" support software provided by DEC. Additional tasks include optimizing the performance of the compiler and conducting a study of the interface between compiler generated microcode and CPU architectures.

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INTRODUCTION

The use of microprogramming, especially for high usage segments of computer programs, as a way to enhance hardware performance has been demonstrated many times (1,2). Since the advent of minicomputers, circa 1970, the manufacturers of these systems have offered their customers a "user" microprogramming option. This consists of a small writable control storage (WCS) and micro assemblers and simulators to support generation of microprograms. There hasn't been a wide acceptance of this "user" microprogramming option by the purchasers of mini-computers primarily because generation of microprograms is an error prone and costly task. The basic support offered the "user" microprogrammer has simply been inadequate to overcome the difficulties of preparing and using microcode.

The purpose of the research described in this report is to develop additional tools to support the "user" microprogrammer. The use of high level languages (HLLs) for expressing computer programs are taken for granted by conventional software programmers and the use of this technique to generate microcode appears promising. Establishing feasibility that HLL compilers can be developed to produce efficient microcode is the main objective of this research activity. Efficient microcode in this context means microcoded routines which significantly enhances hardware performance on critical often used software segments hereafter referred to as kernals.

The research described in this report has been underway for about two years. In the beginning two compilers were available. One produced microcode from the MPL HLL for the INTERDATA Mod 3 and the other generated quadruples from the PLM HLL (3,4) . The INTERDATA Mod 3 was designed with a vertical control word format consisting of 16 bits and four modes. Generating microcode for this machine is in many ways similar to conventional assembly language programming. As was to be

expected, the compiler designed to produce INTERDATA Mod 3 microcode was quite efficient. The big challenge was to produce microcode via a compiler for a computer with a horizontal control word format. A horizontal control word may be from 50 to 100 bits wide and have from 20-40 control fields.

The first research effort in this activity consisted of using the PLM to quadruple compiler to generate microcode for the DEC PDP 11/45 machine (4) . A quadruple to 11/45 microcode translator was developed and performance measured. The results were encouraging which lead to a much more challenging research effort (5) to change both the input to the compiler and to generate microcode for the DEC VAX 11/780 machine which offered a "user" microprogramming option. The input to the compiler was changed from PLM to PASCAL and the output again went via the intermediate quadruple format directly to microcode format of the VAX machine which has a control word consisting of 96 bits with nearly 30 control fields. Unfortunately, at the time of this research effort DEC hadn't released the "user" microprogramming support manuals and this greatly hindered our ability to determine if the microcode generated was correct and to measure its performance.

At the inception of the research effort of this present contract in November 1979, it was decided to transfer the compilers which produce microcode for the VAX machine to be operable on the BMDATC Test Bed VAX systems. A companion ARO contract (6) was established to transport the PASCAL to VAX microcode compiler from the IBM 370 so that it would execute on the VAX system. To do this, the XCOM compiler, which is part of the XPL Translator Writing System, was modified to produce quadruples as an output instead of 370 machine language.

An additional program was written to generate VAX MACRO language statements from the quadruples. This research activity has been slowed by many unusual events including a two month shut down of the Computer Center at GWU along with the necessity to replace the programmers working on the compiler twice. As a result this program fell behind schedule and wasn't able to support some aspects of this research effort.

Another major problem was the long delay in release of the VAX "user" microporgramming support documentation. This material wasn't received until April of '80 which hampered our ability to verify the correctness of the compiled VAX microcode. The combined effect of the two problem areas was to lead to our concentration on the quadruple to VAX microcode portion of the compiler. The PASCAL to quadruple compiler developed under the previous research effort was essentially assumed to work "as is" and the performance optimization and measurement activity concentrated on the quadruple to microcode translator. Fortunately, this approach worked quite well and good estimated performance measurements were obtained. Confirmation of these performance measurements on VAX systems at the BMDATC Test Bed are now underway.

There are four objectives for this research activity. The first was to complete the transfer of the PASCAL to VAX 11/780 microcode compiler to be operational on the BMDATC Test Bed. Achievement of this objective was contingent on the ARO companion effort noted above which has fallen behind schedule. Accordingly, the accomplishment of this objective has also fallen behind schedule. Rapid progress is being made and an operational PASCAL to VAX microcode compiler should be available at the BMDATC Test Bed in the fall of '80. The second objective was to measure the performance of the PASCAL to VAX microcode compiler.

This objective has been largely met with the exception of confirming estimated execution times with actual timing runs on the VAX systems at the BMDATC Test Bed. An attempt to do this failed because of systems software problems within the VAX VMS support software. The third objective was to optimize the PASCAL to VAX microcode compiler performance. Again this activity was concentrated on the quadruple to VAX microcode translator and good results were obtained. The main point here was to transfer data requests to the VAX internal registers to avoid the overhead of main storage references. The fourth objective was to study the interface between the compiler and the hardware microcode. This was done in conjunction with objective 3 and a better understanding of this interface was developed, however, much remains to be done in this research area.

The results obtained from this research effort are mainly to demonstrate that a HLL compiler can produce efficient microcode for the VAX machine. Specific results to be presented later indicate that compiler produced microcode is nearly comparable to microcode produced by hand. This should certainly be the case for the "occasional" microprogrammer who wouldn't develop the skill level that could be obtained by a full-time microprogrammer. Secondly the optimization techniques incorporated in the quadruple to VAX microcode translator work quite well and appear to be applicable to producing microcode for a wide variety of host machine hardwares. Finally a better understanding of the compiler to microcode generation process will lead to the specification of host machines which are better suited for interfacing to high level languages in general.

In view of the results obtained to date in this research activity to produce compilers from HLL's to microcode, it can be concluded the feasibility has been established and progress is being made in reduction-to-practice of this technique.

Adding this tool to the available microprogramming support should make "user" microprogramming a much more worthwhile option for purchasers of hardware with this feature. With the availability of cheaper hardware and the ever increasing cost of software, the use of microprogramming to enhance system flexibility appears to be an attractive advantage. This research activity will lead to better support tools for microprogrammers and ultimately to a wider use of this technique to improve both hardware performance and flexibility.

The final report includes six sections and four appendices. After this introductory section, there follows a section on research objectives and one on research accomplishments. A fourth section deals with compiler performance followed by a section on the HLL compiler hardware interface. The report concludes with a section containing summary comments on the significance of this research and suggestions for follow-on activity.

RESEARCH OBJECTIVES

Before beginning a detailed discussion of the objectives of this research effort, a few preliminaries are in order. The initial activity was to demonstrate the feasibility of producing with a compiler microcode for a computer employing a horizontal control word format. This was demonstrated (4) using the DEC PDP 11/45 as a host machine which has a 56 bit control word with nearly 20 control fields. This research revealed the importance of the compiler hardware interface and especially the necessity of taking advantage of available registers in the host machine to minimize main storage references. The next effort was an extension of the feasibility study to change the simple PLM source language for the compiler to PASCAL and to replace the DEC 11/45 by the VAX 11/780 as the host machine. The VAX 11/780 is a much more complex host machine than the 11/45 and utilizes a 96 bit control word format. Finally a companion effort was initiated to transport the PASCAL to VAX 11/780 microcode compiler to the VAX systems within the BMDATC Test Bed.

The first objective of this research contract was intended to be supportive of the other three and as a follow-on to the ARO contract objectives. By transferring the PASCAL to VAX microcode compiler to be operational at the BMDATC Test Bed, it was hoped that other BMDATC contractors would be encouraged to take advantage of the "user" microprogramming capability of the VAX hardware to enhance their system performance. To support this goal it was necessary to make the PASCAL to VAX microcode compiler available on the BMDATC Test Bed as well as provide support documentation as to how these facilities are to be used. As an initial step in this direction the PASCAL compiler had to be well documented and a "users" manual is required. In addition, the compiler must be made resident on the VAX systems at the BMDATC Test Bed and local systems programming personnel had to be familiarized with how to use this facility.

The second objective was to evaluate the performance of the PASCAL to VAX 11/780 microcode compiler. This would proceed through several phases starting with the relatively unoptimized version available at the inception of this research activity and moving on to the optimized versions of the compiler. The performance of compiler generated microcode would be measured against hand generated microcode and also against versions of the test programs coded in other high level languages available on the VAX system, i.e. mainly FORTRAN IV. Terms of measurement would be in running time and where possible in terms of control storage space utilization.

Objective three would be corollary with objective two in that optimization of the compiler would be carried out to provide better performance against hand coded microprograms and also in terms of running time against versions of the test programs coded in other HLL's resident on the VAX system. This objective has two aspects, namely optimization of the PASCAL to quadruple compiler and optimization of translation of quadruples to microcode. The latter aspect proved to be especially significant in generation of microcode for the PDP 11/45. Fairly standard optimization techniques will be considered in achieving this objective for the PASCAL to quadruple compiler. Register allocation algorithms will be used to the maximum extent possible to optimize the quadruple to VAX microcode translator to improve run time performance and minimize the amount of control store usage.

The fourth objective is to study the interface between the PASCAL to VAX 11/780 microcode compiler and the CPU architecture. While this interface physically is at the microcode level, factors such as internal register availability, HLL features, and the choice of an intermediate representation all play

a role in determining total system performance. The experience gained in generating microcode for the PDP 11/45 from the PLM HLL demonstrated the importance of this objective. In generating test cases, it was discovered that for all but one of the test cases, Fibonacci Series, it wasn't possible to efficiently hand microprogram them because of the shortage of internal registers in the PDP 11/45 CPU. From the extent to which the goals of this objective are reached, we should be better able to determine architectural specifications of host machines to enhance their microprogrammability and ultimately their performance in a wide range of applications.

The four objectives for this research effort which are described above span a wide range of issues in the design of compilers to produce microcode. As in any research effort all objectives aren't equally achieved and as activity progresses new directions may appear and are pursued. Another factor is the research environment which can often lead to decisions to pursue different approaches to avoid obstacles that impede progress in the initially chosen directions. This contract activity encountered many problems and directions were changed to maximize the accomplishments as will be described in the next section.

PROJECT ACCOMPLISHMENTS

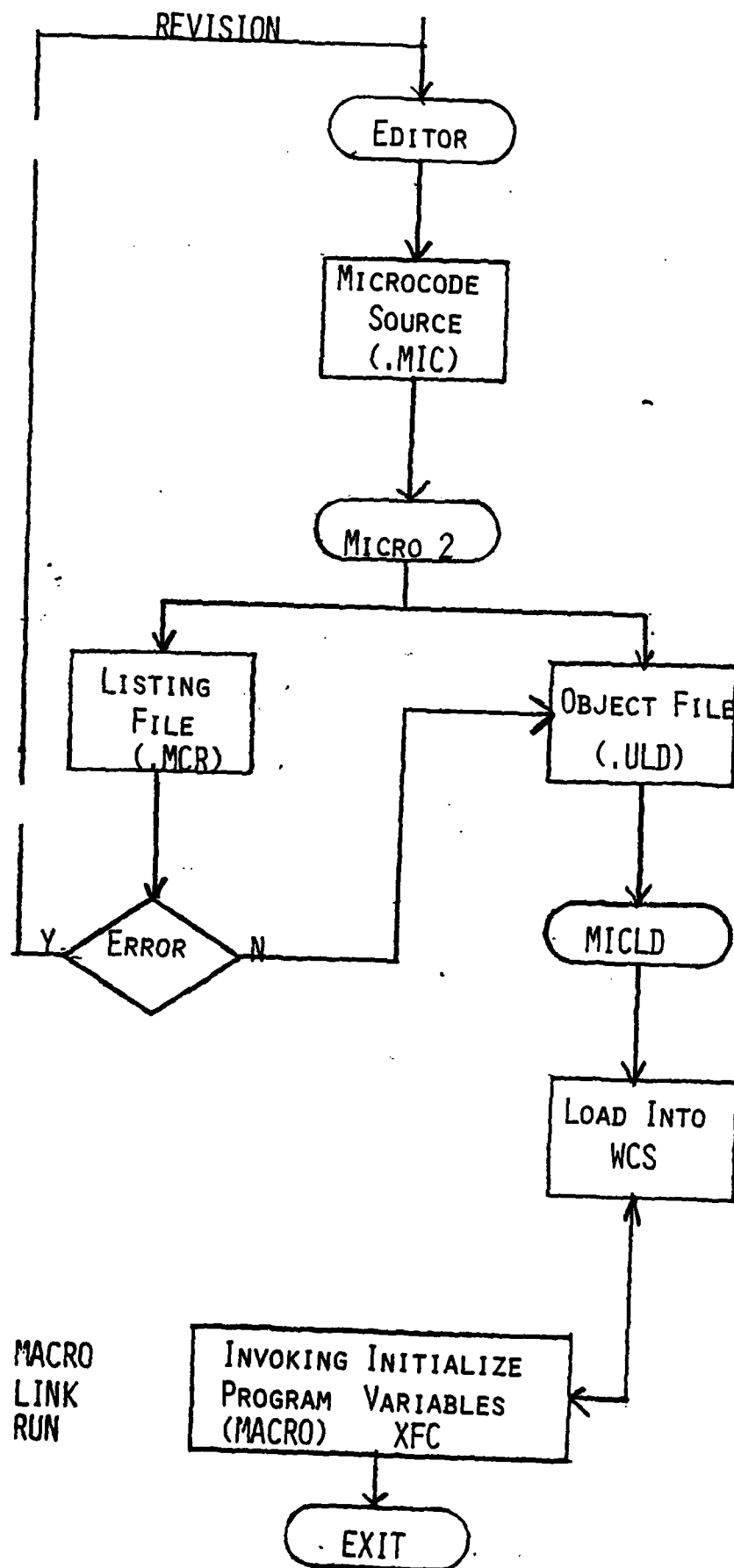
A number of accomplishments have been achieved as a result of the research activity into the design of compilers to convert computational algorithms expressed in a HLL into microcode. Some of the high lights include a high degree of optimization of the efficiency and performance of the microcode produced by the compiler which is executable on the VAX 11/780 CPU. Another significant accomplishment is the greater understanding of the interface between compilers which generate microcode and CPU architectures. As design techniques for microprogrammed CPU's are improved, the interface between the software and firmware and these architectures becomes a more critical technical consideration. While many of the research objectives were met, not all were and in some cases a re-direction was required to compensate for circumstances arising during the research activity.

Two events beyond our control contributed to the degree of accomplishment of the research objectives. The first was the delay until April '80 of the receipt of the complete DEC support documentation on how to microprogram the VAX CPU. Some preliminary and partial information became available in January '80 but lacking the complete documentation adversely affected the quadruple to microcode translator development. The second problem was the shut down of the computer facilities at GWU which were required to support this research. This led to a late start in achieving objective 1 to get the PASCAL compiler operational on the VAX System. A third problem, characteristic of a graduate school research environment, is the high rate of turnover of research staff. This research project was especially hard hit by the necessity of replacing two lead compiler programmers along with the unavoidable training period for replacements.

The accomplishments for each objective will be discussed below. It should be emphasized that this is an ongoing research effort and objectives not entirely achieved at the time this report is being written will be accomplished in the near future. The status of accomplishment for each objective will include an estimated completion date where appropriate.

Progress on objective one to make the PASCAL to VAX 11/780 microcode compiler operable on the BMDATC Test Bed is behind schedule by about two to three months for the reasons noted above. Work on interfacing this compiler with the DEC "User" Microprogramming support documentation is underway. A preliminary user's microprogramming manual has been prepared and is shown at appendix B. Of particular importance is the design of invoking programs which provide an interface between the "user" microprogram and the VMS operating system. An overview block diagram of the invoking procedure is shown in figure 1 and a sample invoking program is shown in figure 2. Another example of "user" documentation intended for operational personnel at the BMDATC Test Bed is shown at appendix A. It is a documented program written in the XPL language which converts quadruples to the VAX system MACRO language along with a variation of this translator which is still in development produces microcode for the VAX 11/780 from quadruples. In summary the status of objective one is that it is only partially complete and behind schedule. While some of the check out of the compiler can be carried out on the VAX 11/780 at GWU, a major effort will also be required at the Test Bed to bring it into operational status there.

Objective two is to evaluate the performance of the PASCAL to VAX 11/780 microcode compiler in terms of operational performance and microcode storage



COMMAND

\$EDIT FILE NAME .MIC

\$MICRO 2 FILE NAME

\$MICLD FILE NAME

FIGURE 1 GENERATION
OF MICROCODE
FOR VAX 11/780

\$ MACRO
\$ LINK
\$ RUN

```

TYPE SORTTEST.MAR
.TITLE SORTTEST
.ENTRY SORTTEST, "M<>"
$CHKRNL_S ROUTIN=SAVEC ;SAVE AND CHANGE XFC VECTOR IN SCB.
$CREATE FAB=OUTFAB
$CONNECT RAB=OUTRAB
$ASCTIM_S ,TIMBUF=ATIMENOW,,
MOVCS #32,ATIMENOW,TIMOUT
$PUT RAB=OUTRAB
MOVAL AR,RO ;STARTING ADDR OF ARRAY
;-----
XFC
;-----
$CHKRNL_S ROUTIN=RSVEC
$EXIT_S
$ASCTIM_S ,TIMBUF=ATIMENOW,,
MOVCS #32,ATIMENOW,TIMOUT
$PUT RAB=OUTRAB
$CLOSE FAB=OUTFAB
;-----
SAVEC: .WORD 0
MOVL SCB$AL_BASE+20,RIVEC
MOVL #2,SCB$AL_BASE+20
RET
;-----
RSVEC: .WORD 0
MOVL RIVEC,SCB$AL_BASE+20
RET
;-----
RIVEC: .PSECT VECTOR, LONG
.LONG 0
.LONG 0
;-----
OUTFAB: $FAB FNM=TIMBF,RFM=FIX,MRS=TIMSIZ,RAT=CR
OUTRAB: $RAB FAB=OUTFAB,RBF=TIMOUT,RSZ=TIMSIZ
TIMOUT: .BLKB 32
TIMSIZ=-TIMOUT
ATIMENOW: .LONG 20%-10%
.LONG 10%
10%: .BLKB 32
20%: .BLKB 0
AR: .BLKL 255
.END SORTTEST
$

```

Figure 2 Microcode Invoking Program in VAX 11/780 MACRO Language

requirements. After getting off to a slow start due to lack of availability of the DEC support documentation for "user" microprogramming, considerable progress has been made in evaluating the compiler performance which looks quite acceptable. One missing detail for this objective is to conduct timing runs of the microcode produced both by hand and by compiler in the VAX systems installed at the Test Bed. An attempt was made to do this but failed due to problems with the VAX system software supporting the timing procedure. The test approach adopted for this objective was to initially code the four test programs in four ways. These are to code the test program in: DEC FORTRAN IV, PASCAL, microcode derived from quadruples, and hand coded microcode. Consideration was given to also coding the test programs in the VAX MACRO language but this was dropped when it became apparent that there would be little improvement in this representation over the MACRO version generated by the FORTRAN IV compiler. Timing tests were made on the FORTRAN IV version of the test programs and estimated execution times were generated for the quadruple and hand coded microcode versions. It is these latter versions that we were unable to get actual running times on the Test Bed VAX systems. Because of the importance of the accomplishments for objective 2, it will be covered in more detail in section four dealing with the compiler performance.

Accomplishments for objective three are corollary to those for objective 2. Optimization of the PASCAL to VAX 11/780 microcode compiler is decomposed into two parts. The first part deals with the PASCAL to quadruple compiler. Because of the problems noted above for objective one, it wasn't possible to make an attempt to significantly improve this compiler performance in a general way. It is also our observation from earlier research experience that significant gains

in microcode operational performance are unlikely to be due to the design of the compiler. Instead in accomplishing objective three all the stress was placed on optimizing the performance of the quadruple to VAX 11/780 microcode translator. Here significant gains in performance were obtained by taking advantage of allocating data to registers and combining quadruples into one microinstruction were possible. This required definition of special microcoded MACROS which is the interface to the "user" microprogrammer supported by the DEC microprogramming documentation. While all aspects of optimizing the generation of microcode from quadruples haven't been investigated, the performance of the microcode generated from quadruples compared to hand coded microcode looks very good. Again because of the significance of our accomplishments for this objective they will be discussed in more detail in section four below.

The study of the HLL compiler CPU interface is an out growth of earlier observations of the critical nature of this boundary between software, firmware and hardware. Even more interesting is the trend, especially apparent in the VAX machine, for CPU architectures to directly reflect HLL representations. Examples include the support of procedures, subroutine calls, stacks, and a host of other HLL features at the machine language level. This leads to direct interpretation of these HLL features at the microcode level and eliminates the necessity of encoding these features in conventional machine language, e.g. the DEC PDP 11 assembly language. This introduction of HLL concepts directly into the machine language of the CPU tends to diminish the advantages of microprogramming computational algorithms to gain run time performance. As will be noted below this is born out by our performance evaluation showing only about 3 to 4 to one advantage

of hand microcoded algorithms over the FORTRAN IV equivalent. This shows the significance of this trend in CPU architecture design. While performance advantages may not be so great in using directly microprogrammed kernels in the VAX system, the flexibility of microprogramming can still offer lots of advantages. To investigate this further requires selection of algorithms which will achieve maximum benefit from microprogramming and evaluate the effectiveness of this representation as opposed to representations generated at the FORTRAN IV or MACRO language level. Again because of the importance of this objective, it is discussed in more detail in section five.

Considerable progress has been made on the objectives originally stated for this research effort in spite of the many obstacles encountered. Much remains to be done and the proposed on-going research addresses many of these issues. Most important, a good foundation is being established utilizing "state-of-the-art" hardware to develop tools to assist in the generation of microcode. With some estimates of the cost of generating a line of microcode running as high as \$1000.00, any improvement in the productivity of microprogrammers can bring about significant savings. In spite of the trend of CPU manufacturers to incorporate HLL features directly in hardware, this flexibility of being able to directly microprogram critical software kernels makes the development of tools to assist the microprogrammer a high priority effort. As more is learned about the compilation procedures for microcode, better advantage can be taken of available hardware performance. It is toward this objective that the long range goals of this research effort are directed.

COMPILER PERFORMANCE

HLL Compiler performance can be measured in many ways. These include: impact on programmer productivity, readability and documentation of source code, computational thruput of the object code produced by the compiler, and amount of storage space required for a compiled program. From these fundamental measures other criteria can be derived including compiler efficiency (7) which is a comparison of computational thruput and storage requirements of an algorithm coded in a HLL and assembly language. To optimize the performance of a compiler, it is common practice to try to reduce the computational time, commonly referred to as "run time" of the generated object code. Optimization of the run time of the object code often requires additions to the time it takes to compile a program. If compile time also is an important factor, then tradeoffs may be required between object code optimization and compiler run time.

In this research project microcode execution time was the goal of the optimization effort. Compile time wasn't considered nor were control storage requirements. As noted before, optimization activity was directed at the quadruple to microcode translator. The main factors to be considered were the allocation of registers to the variables being modified at any particular segment of the program, enablement of branch operations, and accessing data arrays. By careful design of the translator program, we were able to generate microcode which was comparable in run time performance to hand generated microcode.

To test the compiler two approaches were used. The first was to make timing estimates by counting the number of microinstructions that would be executed to carry out the computations required for the test cases. The execution time of each microinstruction, which is typically 200 nonoseconds, were used as factors to

estimate test program run times. The second approach is to create a microprogram load module and actually execute it on the VAX systems in the BMDATC Test Bed. Because of the granularity (10 milliseconds) of the elapsed time measurement facility on the VAX system, it is necessary to run the test case many times in order to be able to make a run time estimate. The control of the number of test cycles to be run must be included within the microcode and this introduces a bias in the run time estimate. There is an additional timing overhead introduced by the invoking program as it passes control to the microprogram. This is a one time bias which doesn't seriously affect the accuracy of the run time tests. In order to reduce the impact of these test errors, the number of test run cycles is varied to obtain an average run time for each test case.

To illustrate the compilation procedure an example is shown in figure 3. This shows a sort routine which sorts an array of numbers into ascending order. This program has a best and worst case test requirement. The best case is when all the elements to be sorted are already in ascending order and the worst case occurs when they are initially all in descending order. It is evident from this figure as to where some overhead is inherent in microcode generated by a compiler. Do loops require indices to be specified and comparisons must be made on iteration variables. For branches and if-then-else constructs it is necessary to compute a predicate before determining whether to go to the branch address or not. In spite of these overhead aspects of compiled microcode, the run time performance of microcode generated from quadruples is nearly comparable to hand generated microcode as is shown below.

The quadruple to microcode translator was designed to produce as efficient microcode as possible. The design approach was to first microcode the test problems by hand and compare it to the microcode derived by translation from quad-


```

        .TITLE "BUBBLE";
        .REGION /1400,17FF;
;BASIC PROGRAM FLOW:--;
;INITIALIZE FILE TO BE SORTED--;
;INITIALIZE SORT PROGRAM VARIABLES IS & K--;
;SET UP OUTER DO LOOP FOR SORT BASED ON INDEX K--;
;SET UP INNER DO LOOP FOR SORT BASED ON INDEX I FOR FILE AR--;
;ON COMPLETION OF SORT PASS ON INNER LOOP AND IS=1--;
;DECREMENT K AND REPEAT INNER LOOP--;
;WHEN K=0 OR IS=0 AT END OF INNER PASS EXIT PROGRAM--;
;INPUT
;      RO AR MEMORY BASE ADDR.
;LABELS
;      ADDR2 START OF SORT K(OUTER) LOOP
;      ADDR3 LAST STMT OF INTERCHANGE LOOP
;      ADDR4 START OF SORT FILE LOAD LOOP
;      ADDR5 INPUT TO SORT INDICE INITIALIZATION
;      ADDR6 BEGIN INTERCHANGE LOOP
;      ADDR7 LAST STMT OF SORT K(OUTER) LOOP
;      ADDR8 EXIT FROM SORT PROGRAM
;INTERNAL VARIABLES
;      I INDEX TO ARRAY AR STORED IN REG 1
;      IS INTERCHANGE SIGNAL STORED IN REG 2
;      ITEMP WORKING SPACE FOR INTERCHANGE PROG. IN REG 3
;      K OUTER SORT LOOP INDEX STORED IN REG 4
;INITIALIZATION OF ARRAY TO BE SORTED
;IT WILL CONSIST OF 255 ELEMENTS IN
;INVERSE ORDER

```

Figure 3 - Example of PASCAL To QUADRUPLE To VAX 11/780
MICRO 2 ASSEMBLY LANGUAGE COMPILATION
PROCEDURE FOR SORT TEST CASE.

QUADRUPLES

VAX
MICRO 2

OPER	OPND 1	OPND 2	OPND 3
AR (1) := 255;	U . . . S0		T14
MOV	# 255		@T1
FOR I: = 2 to 255 DO;	# 2		U . . . S1
ADDR 4			
GT	U . . . S1	# 255	T1
BRT	ADDR 5	T1	
ADD	U . . . S0	U . . . S1	T1
SUB	@ T1	# 1	T2

```

---; Q_RCR0J; AR BASE ADDR TO Q REG
---; RCR5J_ALU,ALU_Q+KC.1J; AR(Q)+1 TO REG 5
---; D_KC.FFJ; 255 TO D REG
---; VA_ALU,ALU_LA,LAB_RCR5J; ADDR AR(1) TO MAI
---; CACHE_DELONGJ; 255 TO AR(1)
---; RCR1J_KC.2J; I=2
---; ADDR4:
---; Q_KC.FFJ; 255 TO Q REG
---; ALU_LA-Q,LAB_RCR1J,CLK.UECC; IS I > 255?
---; ALUT;
---; =1010...J/ADDR5; COMPLETION OF SORT FILE LOG
---; LAB_RCR0J; ADDR OF AR TO AB LATCH
---; Q_RCR1J; PUT INDEX I FOR AR INTO Q REG
---; RCR5J_ALU,ALU_Q+LB; ADDR OF AR(I) TO RS
---; VA_ALU,ALU_LA,LAB_RCR5J; ADDR AR(I) TO MAI
---; DELONGJ_CACHE; AR(I) TO D REG
---; RCR6J_ALU,ALU_D-KC.1J; AR(I)-1 TO REG 6

```

Figure 3-2

ASCA SOURCE	QUADRUPLES				VAX MICRO 2	COMMENT
	OPER	OPND 1	OPND 2	OPND 3		
	SUB	T1	#1	T1	LAB_RCR5J; ADDR OF AR(I) TO AB LATCH RCR5J_ALU,ALU_LA-KC.1J; ADDR OF AR(I-1) TO REG 5	
	MOV	T2		@T1	D_RCR6J; AR(I)-1 TO D REG VA_RCR5J; ADDR OF AR(I-1) TO MAR CACHE_DELONGJ; AR(I)-1 TO STORAGE LAB_RCR1J; I INDEX TO AB LATCH	
) CONTINUE	ADD	U . . .S1	#1	S2	RCR1J_ALU,ALU_A+KC.1J,J/ADDR4; INCREMENT I ADDR5;	
	ADDR 5					
; = 0	MOV	#0		S2	RCR2J_KCZEROJ; SET VAR IS=0 INTERCHANGE SIGNAL RCR4J_ALU,ALU_KC.FFJ; SET VAR K=255	
	MOV	#255		S4	ADDR2;	NUMBER OF ELEMENTS TO BE SORTED;
= K-1	ADDR 2				LAB_RCR4J; K TO AB LATCH	
	SUB	S4	#1	S4	ALU_LA-KC.1J,RCR4J_ALU; K-I TO K	
R I: = 1 To K DO;	MOV	#1		U . . .S1	RCR1J_KC.1J; SET I=1 ADDR6;	
	ADDR 6				Q_RCR4J; K TO Q REG	
	GT	U . . .S4	U . . .S1	T	ALU_LA-Q,LAB_RCR1J,CLK,UBCC; IS K-I>0 ALU7;	
	BRT	ADDR 7	T		=1010 J/ADDR7;	

Figure 3-3

PASCAL SOURCE	QUADRUPLER				VAX MICRO 2	COMMENT
	OPER	OPND 1	OPND 2	OPND 3		
IF AR(I) < AR(I + 1) Then Go to ADDR 3	ADD	U . . . S0	U . . . S1	T1	LAB_RCR0J; BASE ADDR OF AR TO AB LATCH Q_RCR1J; I TO Q REG RCR5J_ALU, ALU_Q+LB; AR BASE ADDR+1 TO REG	
	ADD	#1	T1	T2	LAB_RCR5J; AR(I) TO AB LATCH ALU_LA+KC.1J, RCR6J_ALU; AR(I+1) TO REG 6	
	LT	@T1	@T2	T	VA_RCR6J; ADDR OF AR(I+1) TO MAR DELONGJ_CACHE; AR(I+1) TO D REG Q_D; AR(I+1) TO D REG VA_RCR5J; ADDR OF AR(I) TO MAR DELONGJ_CACHE; AR(I) TO D REG ALU_Q-D, CLK.UBCC; AR(I+1)-AR(I) ALUT;	
	BRT	ADDR 3			J/ADDR3; BR TO END OF EXCHANGE LOOP	
: = 1 EMP: = AR(I)	MOV	#1			RCR2J_KC.1J; SET IS=1 EXCHANGE SWITCH	
	ADD	U . . . S0	U . . . S1	T1	LAB_RCR0J; AR BASE ADDR TO AB LATCH Q_RCR1J; I TO Q REG RCR5J_ALU, ALU_Q+LB; AR(I) TO REGS VA_RCR5J; AR(I) TO MAR DELONGJ_CACHE; AR(I) TO D REG RCR3J_D; AR(I) TO ITEMP (REG3)	
	MOV	@T1		U . . . S3		

Figure 3-4

PASCAL SOURCE	QUADRUPLES				VAX MICRO 2	COMMENT
	OPER	OPND 1	OPND 2	OPND 3		
R (I) := AR(I + 1)	ADD	U . . . S0	U . . . S1	T1	LAB_RCR0J; AR BASE ADDR TO AB LATCH Q_RCR1J; I TO Q REG RCR5J_ALU,ALU_Q+LB; AR(0)+I TO REG 5	
	ADD	T1	#1	T2	LAB_RCR5J; AR(I) TO AB LATCH ALU_LA+KE.1J,RCR6J_ALU; AR(I+1) TO REG 6	
	ADD	#1	T1	T2	LAB_RCR6J; ADDR OF AR(I+1) TO AB LATCH ALU_LA+KE.1J,RCR6J_ALU; AR(I+1) TO REG 6	
	MOV	U . . . S3		@T3	VA_RCR6J; AR(I+1) TO MAR D_RCR3J; ITEMP TO D REG CACHE_DCLONGJ; ITEMP TO AR(I+1)	
CONTINUE DO	ADDR 3				ADDR3;	
	ADD	#1		U . . . S1	LAB_RCR1J; I TO AB LATCH RCR1J_ALU,ALU_LA+KE.1J; I=I+1	
	BR	ADDR6			J/ADDR6; RETURN TO SORT LOOP	
	ADDR 7				ADDR7;	

Figure 3-5

PASCAL SOURCE	QUADRUPLES				VAX MICRO 2	COMMENT
	OPER	OPND 1	OPND 2	OPND 3		
JFK>THEN Go to ADDR 2	GT	U . . . S4	#0	TO	LAB-RER4J; K TO AB LATCH	
					ALU_LA-KCZER0J,CLK,UBCC; IF K-0=0 THEN BR TO ADDR2; ;K-0 BR TO ADDR2 IF LESS THAN;	
	BRT	ADDR 2			ALU?; IS THERE AN ALU OUTPUT	
					#1010 J/ADDR2;	
END	END				PC_PC+1,CLR,IB,OPC,J/062; END OF BUBBLE	

Figure 3-6

ruples. The differences were examined and the translator was modified to reduce this difference to the maximum extent possible. In some cases this involves changing the quadruple input from the PASCAL to quadruple compiler. Changes are being made to the compiler to produce the desired quadruples.

A final effort, which is currently in process, is to redefine the MICRO 2 MACROS to better reflect the translation of quadruples into microcode. The MICRO 2 MACROS are a set of micro assembly language routines which are used by DEC Engineers in the design of the microprograms to interpret the VAX machine instructions set. Several instances have been detected where new MICRO 2 MACRO definitions would offer still better hardware performance for microcode generated from quadruples.

A major consideration in the design of both the PASCAL to quadruple compiler and quadruple to microcode translator are precise definitions of the quadruple formats and specifications in terms of MICRO 2 MACROS of each quadruple type. The quadruple consists of an operation, two source operands, and a destination operand. Each operand can be expressed in terms of different data types. This gives an extremely wide range of quadruple formats and data definitions. Appendix C lists the basic quadruple formats along with a representative set of quadruple types. Note that for each operator there are a number of potential operand data types leading to a wide variety of quadruples.

Appendix D contains a table showing the MICRO 2 MACROS required to implement the various quadruple types. Again a given quadruple operator may have a number of MICRO 2 MACRO representations corresponding to various operand data

types. Finally in appendix E a couple representative microcoded test cases are shown. Some of these as indicated are derived from quadruple representations and some are representative of hand coded microcode.

The data obtained for the estimated run times is shown in table I. In general the microcode produced by the PASCAL compiler had a run time which averaged 45% longer than the run time of the equivalent hand generated microcode. The same test problems coded in DEC FORTRAN IV and actually timed on the VAX system had an average run time which was 312% longer than the hand generated microcode. The average speed advantage of the PASCAL to microcode compiler over the FORTRAN compiler is 2.22 to one. This result is a little surprising since in general going directly to microcode should produce a bigger speed advantage. Part of the reason is the inclusion of high level language instructions in the VAX 11/780 instruction set which facilitates the direct interpretation of a HLL on the VAX system. This issue will be more extensively discussed in the next section.

From the data in table I, we can conclude that the PASCAL to microcode compiler is an effective software development tool. It produces quite efficient microcode which is nearly as efficient as the computational performance of hand generated microcode. The optimization effort on the quadruple to microcode translator was quite successful as is evidenced by the efficiency of the microcode produced. Further effort should be expended on the quadruple to microcode translator to see if its performance can be improved still further.

TEST CASE COMPILER	GREATEST ELEMENT (10)	FIBONACCI (40)	PRIME (250)	BUBBLE SORT (250)	
				WORST	BEST
HAND CODED MICROCODE	28.19	64.06	1400	.14x10 ⁶	.06x10 ⁶
PASCAL TO QUAD TO MICRO 2	37.09	100	1700	.26x10 ⁶	.08x10 ⁶
FORTTRAN	90	200	5000	.36x10 ⁶	.19x10 ⁶

TABLE 1
PERFORMANCE COMPARISON
PASCAL TO MICROCODE COMPILER

ALL TIMES IN MICROSECONDS

HIGH LEVEL LANGUAGE-HARDWARE INTERFACE

Interest in the interface between the HLL compiler and the CPU hardware developed during the first phase of this research activity (4) when it was demonstrated that microcode could be generated for CPU's with a horizontal control word format. Because of the inherent machine independence of most HLLs, it was necessary to introduce some intermediate representation which was also relatively machine independent but could be translated into efficient microcode. Quadruples were selected for this representation but other choices could be made, e.g. triples, polish notation, or tree structures. Many of these alternate choices imply the use of a push down stack to implement the translation into microcode.

The selection of quadruples as an intermediate representation was largely motivated by the availability of a compiler which produced quadruples from the PLM language. While quadruples are relatively machine independent, in many ways they are equivalent to machine language. Quadruples are directly interpreted in microcode just as machine instructions are. The basic difference is that machine instructions deal with specific entities within the CPU, e.g. registers, constant generators, shifters, and data formats. Quadruples on the other hand specify only operations and operand types and addresses. These must first be translated into a format more representative of the CPU architecture before being converted into microcode. The translation from quadruples to a similar but machine dependent format is the basic task of the quadruple to microcode translator. Interpretation of the machine dependent quadruple representation is relatively straight forward.

A significant difference between the VAX 11/780 and the PDP 11/45 CPUs is the inclusion of HLL constructs in the machine language of the VAX system. As

noted above this significantly improves the VAX 11/780 system performance in executing algorithms expressed in a HLL which can be translated directly into these machine language expressions. Another feature of the VAX 11/780 machine instruction set is its rich variety of operand formats. This permits literally thousands of different instructions to be generated from only a couple hundred basic types. On the one hand this presents a serious problem to the compiler designer who must attempt to use all the available CPU facilities. The price paid for all this flexibility is longer run time and storage space being required for the compilation procedure. On the other hand the run time performance of compiled machine code begins to approach that of hand generated microcode.

Tradeoffs must be made by the CPU designers to provide features which makes the hardware perform efficiently when most of the software to be executed is originally expressed in a HLL. One danger, of course, is to create a machine instruction set which is too biased towards a particular HLL. This doesn't appear to be the case for the VAX 11/780 but this will be better known when performance data becomes available for HLL compilers for languages other than FORTRAN IV i.e., PASCAL, ADA, and C language which produce object code for the VAX system become available.

Of particular significance to the generation of efficient microcode from quadruples is the availability of registers to the microprogrammer. The VAX 11/780 has seven general purpose registers available at both the machine instruction and microprogram level. In addition there are sixteen scratch pad registers available to the microprogrammer. This is a vast improvement over the registers available in the PDP 11/45 where there were only six general purpose registers available both to the machine language programmer and microprogrammer. Lack of registers made array access very difficult and inefficient in the PDP 11/45 and prevented efficient hand microcoding of most of the test cases used in this research effort. Array manipulations can be easily handled within the VAX CPU and this leads to

significant increases in run time performance of algorithms requiring array accesses.

For a given set of registers, the allocation of data to registers is the critical factor in achieving optimization of translating quadruples into microcode. The procedure is to scan through the quadruples and as operands involving data or addresses are identified, an assignment is made to an available register. If no register is available, then a deallocation algorithm must decide which data item should be removed from the registers. These functions are all carried out at compile time and don't impact the run time performance of the microprogram load module except to the extent that data allocation to registers requires shifting data back and forth between main storage and the CPU registers.

Another key factor in generating microcode is the available data paths within the CPU. Any operation on data for a particular microinstruction requires that the data flow within the CPU is on separate data busses. Determining whether this is the case is a very tedious and error prone procedure. Fortunately the MICRO 2 microcode assembler does a good job of detecting data path usage conflicts and provides error messages to the microprogrammer. The tendency in the design of early minicomputers was to minimize the number of available data paths which had a severe impact on CPU performance. The VAX 11/780 CPU includes enough data paths to mostly avoid having to generate additional microinstructions to resolve data path conflicts. Some improvements could be made in the VAX data path structure but in general, the available data paths are more than adequate to support the other internal processing functions in the CPU.

In summary then the main factors in the compiler to CPU interface are: available machine instructions which directly reflect HLL structure, the supply of registers to permit storage of most of the active computation variables, and provision of adequate data path capacity to avoid having to generate additional microinstructions to resolve data path conflicts." The VAX 11/780 addresses these issues to a much better degree than did the PDP 11/45. As a result the run time performance of HLL compiler generated machine language and microcode approach the performance obtainable from hand coded microcode. Based upon these observations, more study of the compiler CPU interface should be carried out to determine more optimum designs for both the hardware and the compilers.

CONCLUSION

The overall research objectives of this contract were met except where uncontrollable circumstances intervened. A design has been achieved of a PASCAL to VAX 11/780 microcode compiler which produces efficient microprograms and the basic problems of interfacing this compiler to the VAX operating system have been solved. Preliminary support documentation has been prepared to support the "user" microprogramming option for the VAX system by other users of the BMDATC Test Bed.

Because of the efforts to optimize the performance of the PASCAL to microcode compiler, a much better understanding of the interface between a HLL and the microcode control of the CPU was developed. In particular algorithms to achieve optimum use of the registers to store run time variables were of especial interest and importance. The understanding gained of the generation of microcode from compilers can lead to significant improvement in productivity of microprogrammers and expand the capability for the use of this performance enhancing facility.

A further outgrowth of this research effort is the building of a broad base for future research into the techniques of enhancing computer performance thru microprogramming. Of particular significance is the development of host machine register assignment routines and the invoking programs required to pass control to and from the "user" microprogram. With these and other accomplishments, the foundation has been laid for a broad based research effort to develop and perfect support tools for the microprogramming activity.

While much has been accomplished, future research is required to develop techniques for enhancing the flexibility of microcode compilers by demonstrating that they can be converted at the input HLL interface to accept new computer

languages and at the host machine interface to demonstrate they can produce microcode for new host machines. This presents a severe challenge to researchers in this field and much fundamental work remains to be accomplished. The payoff from this research can be the ability to make better use of microprogramming both to enhance the computational performance of a given host machine and make it more flexible with regard to implementation of special purpose computational algorithms.

The research activity described in this final report was participated in by several individuals at The George Washington University. In particular I want to acknowledge the efforts of Robert Jones who did this original layout of the PASCAL and revised XCOM compilers. Mohamoud Ketabchi and Abdol Chenari continued the compiler development and were later joined in this activity by Mr. Kwang. Mr. Teh-Hsin Yang carried out the compiler optimization and evaluation effort.

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Appendix A

- A1 Quadruple To VAX 11/780 MACRO Language Translator
Showing Documentation in Terms of Comments for Each
Procedure
- A2 Quadruple To VAX 11/780 Microcode Translator with
Example of Microcode Derived from Quadruples for
Fibonacci Test Case.

[illegible]

```

190 / * THIS PROCEDURE IS TO PROCESS 'U' TYPE OPERAND. FIRST THE PROCEDURE
191 / * IDENT_INDEX IS CALLED TO SEE IF IT IS INDEXED (I.E. HAS A 'U' SUFFIX)
192 / * AND IF NOT, THEN THE INDEX_OP IS ASSIGNED TO THE OPND AND AND*/
193 / * IDENT_INDEX IS SET TO THE OPND. IF IT IS NOT, CALL PROCEDURE SEARCH_TYPE TO
194 / * EXAMINE THE DATA TYPE OF THE OPERAND AND IF THE FLAG AFI_INDEX=1 AND
195 / * INDEXED_OP=OPND, THEN GENERATE AN INDEXED REGISTER TO THE OPERAND AND RESET*/
196 / * THE FLAG TO ZERO.
197 / *
198 IDENT_INDEX:=PROCEDURE(OPND);
199 DECLARE INDEX_OP CHARACTER, OPND BIT(18);
200 IF BYTE(OPND)=BYTE('U') THEN
201 DO;
202 INDEX_OP:=SRCM_INDEX(OPND,INDEX);
203 IF INDEX_OP=? THEN
204 DO;
205 OPND:=INDEX_OP;
206 OPND:=R;
207 END; / * OF IF THEN DO * /
208 ELSE DO;
209 OPND:=SEARCH_TYPE(OPND);
210 IF (AFI_INDEX=1) & (INDEXED_OP=OPND) THEN
211 DO;
212 OPND:=OPND||('||INDEX_REG||');
213 AFI_INDEX:=0;
214 INDEX_REG:=;
215 END; / * OF IF THEN DO * /
216 END; / * OF ELSE DO * /
217 END; / * OF IF THEN DO * /
218 END IDENT_INDEX;
219 / *
220 / * PROCEDURE IDENT_OPX
221 / * L4
222 / *
223 / * OPX# IS OPERAND NUMBER 1,2,3.
224 / * TMP_OP(3) IS AN ARRAY OF 4 ELEMENTS WHICH ARE INITIALLY 'T0','T1','T2',
225 / * 'T3'.
226 / * THE SYMBTAVL PROCEDURE OPERATES ON EACH OPERAND FROM THE QUAD SPECIFIED
227 / * 'QUANTUM'. NUMBER OF OPX(1,2,3) SELECTS A PARTICULAR OPERAND STORED IN OPND.
228 / * THE THREE MAIN IF STATEMENTS DETERMINE WHETHER THE FIRST CHARACTER OF THE
229 / * OPERAND IS 'U', 'T', OR 'R'. IF IT IS 'U', THEN PROCEDURE IDENT-UTOPX IS
230 / * CALLED. IF IT IS 'T', OPND IS COMPARED TO TMP_OP TO SEE IF IT IS 'T0','T1',
231 / * 'T2' OR 'T3'. IF IT IS 'R', A REGISTER IS GENERATED BY USING FILE DIGIT AND THE
232 / * LETTER 'R' IS CONCATENATED WITH OPND AND OPXCT IS SET TO 'R'. IF THE FIRST
233 / * CHARACTER IS 'R', THEN OPXCT IS SET TO 'R'.
234 / *
235 IDENT_OPX:=PROCEDURE(OPND);
236 DECLARE (OPND,1) BIT(18),TMP_OP(3);
237 / * TAKES OPND AND FINDS ITS TYPE FROM NAME & CTYPE TABLES OR
238 / * ATTRIBUTES TYPE IF IT IS # OR T TYPE * /
239 DO CASE OPND;
240 OPND:=SYMBTAVL(OPND); / * OPX IS 1ST OPERAND * /
241 OPND:=SYMBTAVL(OPND); / * OPX IS 2ND OPERAND * /
242 OPND:=SYMBTAVL(OPND); / * OPX IS 3RD OPERAND * /
243 END; / * OF CASE STATEMENT * /
244 IF BYTE(OPND)=BYTE('U') THEN
245 CALL IDENT_INDEX(OPND);
246 IF BYTE(OPND)=BYTE('T') THEN / * OPERAND IS AT TYPE SYMBOL * /
247 DO;
248 DO I=0 TO 3;
249 IF OPND=TMP_OP(I) THEN GEN_REG:=SUBSTR(DIGIT,I+3,1);
250 END; / * OF DO * /
251 OPND:=R||GEN_REG;
252 OPND:=R;

```

C14 = 228.

CASE 0.
CASE 1.
CASE 2.

C15 = 227.

C16 = 3.


```

388 | IF (OP1(QNUM)=QOP3(QNUM+1)) THEN INDEXED_OP#=2; /* 3ST OPERAND IS INDEXED */
389 | T_INDEX=1;
390 | END LOC_INDEX;
391 | /*****
392 | /*
393 | /*
394 | /*
395 | /* THE PROCEDURE IS TO CONVERT THE QUAD INTO MOVE STATEMENT IN VAX
396 | /* INSTRUCTION. FIRST EXAMINE TO SEE IF THE 1ST AND 3RD OPERANDS ARE IN THE
397 | /* SAME DATA TYPE BY IDENTIFYING THE TWO OPERANDS, IF SO, GENERATE A
398 | /* CORRESPONDING 'MOVE' INSTRUCTION. IF IT IS NOT, INSERT A 'CONVERT'
399 | /* INSTRUCTION TO CONVERT THE 1ST OPERAND INTO THE DATA TYPE OF 3RD OPERAND,
400 | /* THEN GENERATE THE 'MOVE' INSTRUCTION.
401 | /*****
402 | PROC_MOVE=PROCEDURE;
403 | DECLARE (OP1,OP3) CHARACTER; /* IDENTIFY 1ST OPERAND */
404 | CALL IDENT_OPX(0);
405 | OP1=OPND;
406 | OP1CT=OPXCT;
407 | CALL IDENT_OPX(2); /* IDENTIFY 3RD OPERAND */
408 | OP3=OPND;
409 | OP3CT=OPXCT;
410 | IF (OP3CT='R') & (OP1CT='R') THEN /* CONVERT OP1 TO TYPE OF OP3 */
411 | DO;
412 | GEN_REG='2';
413 | CALL CONV_DATA(OP1CT,OP3CT,OP1,'2');
414 | OP1='R2';
415 | END; /* OF THEN DO */
416 | IF OP3CT='R' THEN
417 | DO;
418 | IF (OP1CT='R') & (OP1CT='R') THEN OP3CT='W';
419 | ELSE OP3CT=OP1CT;
420 | END; /* OF IF THEN ELSE */
421 | VOPERAT='MOV' & OP3CT;
422 | VOPRND=OP1 & OP3;
423 | CALL STOR_VAX_INSVOPRAT,VOPRND,QNUM,#OF_GVINSI;
424 | END PROC_MOVE;
425 | /*****
426 | /*
427 | /*
428 | /*
429 | /*
430 | /* THE PROCEDURE IS TO DETERMINE WHETHER THE QUAD IS THE END OF THE PRO-
431 | /* GRAM, IF THE 'QIDBUF' OF THE NEXT QUAD IS '75', THEN GENERATE A 'RET' VAX
432 | /* INSTRUCTION. ELSE, GENERATE A 'POP' VAX INSTRUCTION.
433 | /*****
434 | PROC_UNST=PROCEDURE;
435 | DECLARE SYMBOL CHARACTER;
436 | /* CHECK TO SEE IF NEXT QUAD IS RET */
437 | IF QIDBUF(QNUM+1)='75' THEN
438 | DO;
439 | SKIP_NEXT_QUAD=1;
440 | CALL STOR_VAX_INSV('RET',' ',QNUM,#OF_GVINSI);
441 | END; /* NEXT QUAD IS NOT RETN */
442 | ELSE DO; /* NEXT QUAD IS NOT RETN */
443 | SYMBOL=SYMBTAYL(23P3(QNUM));
444 | CALL STOR_VAX_INSV(SYMBOL,' ',QNUM,#OF_GVINSI);
445 | END; /* OF ELSE DO */
446 | END PROC_UNST;
447 | /*****
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7428 PROC_THOP_ARITH
7470 PROC_THOP_ARITH
7470 PROC_THOP_ARITH
7596 PROC_THOP_ARITH
7612 PROC_THOP_ARITH
7612 PROC_THOP_ARITH
7684 PROC_THOP_ARITH
7724 PROC_THOP_ARITH
7760 PROC_THOP_ARITH
7766 PROC_ARITH
7772 PROC_ARITH
7782 PROC_ARITH
7790 PROC_ARITH
7798 PROC_ARITH
7924 PROC_ARITH
7936 PROC_ARITH
7944 PROC_ARITH
8002 PROC_ARITH
8084 PROC_ARITH
8096 PROC_ARITH
8104 PROC_ARITH
8148 PROC_ARITH
8156 PROC_ARITH
8156 PROC_ARITH
8196 PROC_ARITH
8204 PROC_ARITH
8212 PROC_ARITH
8262 PROC_ARITH
8254 PROC_ARITH
8380 PROC_ARITH
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8396 PROC_ARITH
8436 PROC_ARITH
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8634 LABL_ADDR
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SURENT_ADDR
8640 SURENT_ADDR
8652 SURENT_ADDR
8668 SURENT_ADDR
8692 SURENT_ADDR
8732 SURENT_ADDR
8744 SURENT_ADDR
8752 SURENT_ADDR

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545 | /***** PROCEDURE ALLOCATION *****/
586 | /*
587 | /*
588 | /*
589 | /* THIS PROCEDURE IS TO DEFINE A STORAGE OR A CONSTANT IN VAX ASSEMBLY
590 | /* LANGUAGE. THE LABEL IS GENERATED BY 'STYPE' OR 'STYPE' WHICH IS A PARAMETER PASSED BY
591 | /* 'IS' GENERATED BY EITHER 'BTYPE' OR 'STYPE' WHICH IS A PARAMETER PASSED BY
592 | /* THE CALLING PROCEDURE. THE OPERAND FILED IS GENERATED BY EITHER THE 2ND OR
593 | /* GENERATED BY THE 2ND OPERAND IN NEXT QUAD. IF IT IS PRODUCED BY 'STYPE', IT IS
594 | /* 3RD OPERAND OF THE NEXT QUAD. IF OPERATOR IS PRODUCED BY 'BTYPE', IT IS
595 | /* 'IS' GENERATED BY THE 3RD OPERAND IN NEXT QUAD. AFTER THE CONVERSION. THE
596 | /* LABEL AND DATA TYPE ARE STORED FOR FUTURE USE.
597 | /*****
598 | ALLOCATION:PROCEDURE(BTYPE,STYPE);
599 | DECLARE (BTYPE,STYPE,SYMBOL,SUBS) CHARACTER;
600 | SKIP_NEXT_QUAD=1; /* TWO QUADS ARE PROCESSED */
601 | SYMBOL=SYMBTAYL(QOP1(QNUM));
602 | VLABEL_FLD(DECL)=SYMBOL(1:2);
603 | IF BYTE(QOP3(QNUM+1),1)=BTYPE(1) THEN /* SYMBOL DOES NOT HAVE INIT VALUE */
604 | DO;
605 | VOPERAT_FLD(DECL)=BTYPE;
606 | VOPRND_FLD(DECL)=SYMBTAYL(QOP2(QNUM+1));
607 | END; /* OF IF THEN DO */
608 | ELSE DO; /* VARIABLE HAS INITIAL VALUE */
609 | VOPERAT_FLD(DECL)=STYPE;
610 | SUBS=SUBSTR(QOP3(QNUM+1),1,1); /* DISCARD # */
611 | VOPRND_FLD(DECL)=SYMBTAYL(SUBS);
612 | END; /* OF ELSE DO */
613 | /* STORE SYMBOL NAME AND ITS DATA TYPE FOR FUTURE USE */
614 | NAME(DEF_DEFSYMB)=SYMBOL;
615 | CTYPE(DEF_DEFSYMB)=SUBSTR(STYPE,1,1);
616 | DEF_DEFSYMB=DEF_DEFSYMB+1;
617 | DECL=DECL+1;
618 | END ALLOCATION;
619 | /*****
620 | /*
621 | /*
622 | /*
623 | /* THIS PROCEDURE PROCESSES THE BRANCH ON GREATER THEN. FIRST IDENTIFY THE
624 | /* 2ND AND 3RD OPERANDS. IF THEY ARE NOT THE SAME DATA TYPE, CONVERT 2ND
625 | /* OPERAND TO THE TYPE OF 3RD OPERAND BY INSERTING A 'CONVERT' INSTRUCTION.
626 | /* THEN GENERATE A 'COMPARE' INSTRUCTION. FINALLY PROCEDURE 'GLABL' IS CALLED
627 | /* TO ASSIGN A LABEL TO THE BRANCH ADDRESS. A 'BGR' INSTRUCTION IS GENERATED.
628 | /*****
629 | PROC_BG: PROCEDURE;
630 | DECLARE (OP2,OP3,OP1) CHARACTER, QUAD# FIXED, NOCONV BIT(8) INITIAL(0);
631 | CALL IDENT_OPX(1); /* IDENTIFY 2ND OPERAND */
632 | OP2=OPND;
633 | OP2CT=OPXCT;
634 | IF OP2CT='R' THEN NOCONV=2;
635 | CALL IDENT_OPX(2); /* IDENTIFY 3RD OPERAND */
636 | OP3=OPND;
637 | OP3CT=OPXCT;
638 | IF OP3CT='R' THEN NOCONV=3;
639 | IF (NOCONV=0) & (OP3CT='R') THEN
640 | IF (OP2CT=OP3CT) & (OP2CT='R') THEN /* CONVERT OP1 TO TYPE OF OP3 */
641 | DO;
642 | GEN_REG#='2';
643 | CALL CONV_DATA(OP2CT||OP3CT,OP2,'2');
644 | OP2='R2';
645 | END; /* OF IF THEN DO */
646 | IF (OP3CT='R') || (OP3CT='B') THEN
647 | DO;
648 | IF (OP2CT='R') & (OP2CT='B') THEN OP3CT=OP2CT;

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C21 = 16777215.

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652 | VOPRD=0P211',1113P3;
653 | CALL STOR_VAX_INSVOPRAT,VOPRND,QNUM,0DF_GVINS);
654 | _ABL=GLAB(QOPIONUM);
655 | CALL STOR_VAX_INSVBGR',DLABL,QNUM,0DF_GVINS);
656 | END PROC RG;
657 | /*****
658 | /* PROCEDURE PROC_BR
659 | /* L3---2---1
660 | /*
661 | /* PROC_BR PROCEDURE PASSES THE 1ST OPERAND OF QUAD TO PROCEDURE 'GLABL'
662 | /* TO PRODUCE A LABEL FOR VAX BRANCH INSTRUCTION.
663 | /*****
664 | PROC_BR:PROCEDURE;
665 | DECLARE DLABL CHARACTER;
666 | DLABL=GLAB(QOPIONUM);
667 | /* FILL THE OUTPUT FILE */
668 | CALL STOR_VAX_INSVBGR',DLABL,QNUM,0DF_GVINS);
669 | END PROC_BR;
670 | /*****
671 | /* PROCEDURE SRCH_FBRDESO
672 | /* L3---1---1
673 | /*
674 | /* INPUT PARAMETER 'FQNUM' IS EQUAL TO 'QNUM' WHICH IS EQUAL TO THE NUMBER
675 | /* OF QUADS BEING PROCESSED BY PROCEDURE 'DRIVER'. IF THE 'FQNUM' IS ONE
676 | /* ELEMENT IN THE ARRAY 'FBRDESO()', THEN SET 'FOUND' EQUAL TO 1 AND RETURN
677 | /* IT TO CALLING PROCEDURE, OTHERWISE RETURN -1.
678 | /*****
679 | SRCH_FBRDESO:PROCEDURE(FQNUM) BIT(8);
680 | /* SEARCHES LABEL NUMBER OF THE REFERENCED QUAD */
681 | DECLARE I BIT(8),FQNUM FIXED, FOUND BIT(1);
682 | I=0;
683 | FOUND=0;
684 | DO WHILE IFOUND=0&&I<FBRDESO_IND);
685 | IF FBRDESO(I)=FQNUM THEN FOUND=1;
686 | I=I+1;
687 | END; /* OF DO WHILE */
688 | IF FOUND THEN RETURN I-1;
689 | ELSE RETURN -1;
690 | END SRCH_FBRDESO;
691 | /*****
692 | /* PROCEDURE MISC
693 | /* L2---3---9
694 | /*
695 | /* THIS PROCEDURE PROCESSES MISCELLANEOUS OPERATIONS.
696 | /*****
697 | MISC:PROCEDURE(QINGRP);
698 | DECLARE QINGRP FIXED;
699 | DO CASE QINGRP:
700 | /* CALL PROC_NAME: /* CASE 0 */
701 | OUTPUT=0;
702 | /*
703 | CALL PROC_PUSH: /* CASE 1 */
704 | OUTPUT=1;
705 | /*
706 | CALL PROC_POP: 0 * CASE 2 */
707 | OUTPUT=2;
708 | /*
709 | CALL PROC_HALF: /* CASE 3 */
710 | OUTPUT=3;
711 | /*
712 | CALL PROC_LINK: /* CASE 4 */
713 | OUTPUT=4;
714 | CALL STOR_VAX_INSVRET',0,QNUM,0DF_GVINS);
715 | /

```

9450 PROC_BG
9490 PROC_BG
9926 PROC_BG
9950 PROC_BG
9986 PROC_BG
9992

9992 PROC_BR
10004 PROC_BR
10028 PROC_BR
10028 PROC_BR
10064 PROC_BR
10070

10070 SRCH_FBRDESO
10070 SRCH_FBRDESO
10082 SRCH_FBRDESO
10088 SRCH_FBRDESO
10094 SRCH_FBRDESO
10164 SRCH_FBRDESO
10198 SRCH_FBRDESO
10212 SRCH_FBRDESO
10220 SRCH_FBRDESO
10250 SRCH_FBRDESO
10268 SRCH_FBRDESO
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10274 MISC
10286 MISC
10310 MISC
10310 MISC CASE 0.
10338 MISC
10338 MISC
10338 MISC CASE 1.
10376 MISC
10376 MISC
10376 MISC CASE 2.
10414 MISC
10414 MISC
10452 MISC CASE 3.
10452 MISC
10452 MISC CASE 4.
10490 MISC CASE 5.
10532 MISC

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717 CALL PAUC_UNST; /* CASE 7 */
718 END; /* OF CASE STATEMENT */
719
720 END MISC;
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THIS PROCEDURE IS TO CHECK TO SEE IF THE QIDRUF=60, THEN CALL PROC_MOV
 TO PROCESS THE CONVERSION OF MOVE STATEMENT. IF IT IS EQUAL TO 61, PRINT
 QIDBUF IS 61, NOT IMPLEMENTED YET. IF IT IS 62, CALL PROC_IND
 PROCEDURE.

MOVE_CONV:PROCEDURE(QINGRP);
 DECLARE QINGRP BIT(8);
 DO CASE QINGRP;
 CALL PROC_MOV;
 OUTPUT=QIDRUF IS 61, NOT IMPLEMENTED YET;
 CALL PROC_IND;
 END; /* OF CASE STATEMENT */
 END MOVE_CONV;

PROCEDURE LOGIC_OP
 L2---3--7

LOGIC_OP:PROCEDURE(QINGRP);
 DECLARE QINGRP BIT(8);
 DO CASE QINGRP;
 /*
 CALL PROC_AND;
 OUTPUT=13;
 /*
 CALL PROC_OR;
 OUTPUT=12;
 /*
 CALL PROC_CMPL;
 OUTPUT=11;
 /*
 CALL PROC_XOR;
 OUTPUT=10;
 CALL COMP_CHKBR(QINGRP-4);
 CALL COMP_CHKBR(QINGRP-4);
 CALL COMP_CHKBR(QINGRP-4);
 CALL COMP_CHKBR(QINGRP-4);
 CALL COMP_CHKBR(QINGRP-4);
 CALL COMP_CHKBR(QINGRP-4);
 END; /* OF CASE STATEMENT */
 END LOGIC_OP;

PROCEDURE SHIFT_OP
 L2---3--6

THIS PROCEDURE IS TO CONVERT SHIFT INSTRUCTION OF QUAD INTO
 MULTIPLICATION OF VAX INSTRUCTION. THE OPERATOR IS DECIDED BY THE TYPE OF
 SECOND OPERAND OF QUAD. IF IT IS B-TYPE, THEN OPERATOR IS 'MULB3'. IF IT IS
 M-TYPE, THEN THE OPERATOR IS 'MULB3'. IF IT IS R, #, OR L-TYPE, THEN
 OPERATOR IS 'MULB3'.

SHIFT_OP:PROCEDURE(QINGRP);
 DECLARE (QINGRP,SHIFT,SIZ,1) BIT(8),MULTIPLIER FIXED;
 (QINGRP,SHIFT,SIZ,1) CHARACTER;
 MULTIPLIER=1;
 CALL IDENTIFY_2ND_OPERAND /*
 OP2=QINGRP;

MISC CASE 6.
 MISC CASE 7.
 MISC
 MOVE_CONV
 MOVE_CONV
 MOVE_CONV
 MOVE_CONV CASE 0.
 MOVE_CONV CASE 1.
 MOVE_CONV CASE 2.
 LOGIC_OP
 LOGIC_OP
 LOGIC_OP
 LOGIC_OP
 LOGIC_OP CASE 0.
 LOGIC_OP CASE 1.
 LOGIC_OP CASE 2.
 LOGIC_OP CASE 3.
 LOGIC_OP CASE 4.
 LOGIC_OP CASE 5.
 LOGIC_OP CASE 6.
 LOGIC_OP CASE 7.
 LOGIC_OP CASE 8.
 LOGIC_OP CASE 9.
 SHIFT_OP
 SHIFT_OP
 SHIFT_OP
 SHIFT_OP
 SHIFT_OP

[illegible]

[illegible]

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916 / *
917 / *
918 / * SQUADS# IS THE NUMBER OF QUADS TO BE PROCESSED.
919 / * THIS PROCEDURE IS TO INDIVIDUALLY PROCESS THE QUADS. THERE ARE EIGHT
920 / * PROCEDURES TO BE CALLED TO CONVERT EACH QUAD INTO VAX INSTRUCTION BASED ON
921 / * DIFFERENT TYPE OF QUADS SHOWN BY THE INDEX NUMBER--QIDBUF.
922 / *
923 / * DRIVER:PROCEDURE(SQUADS#);
924 / * DECLARE SQUADS# FIXED;
925 / * DO QNUM=0 TO SQUADS#-1;
926 / * IF QIDFLG(QNUM)=1 THEN CALL FBRLABL_GEN(QNUM);
927 / * IF SKIP_NEXT_QUAD=0 THEN
928 / * DO; / * IF SKIP_NEXT_QUAD IS TRUE THEN QUAD HAS ALREADY BEEN PROCESSED
929 / * NVAL_OF_QID=CONVERT_TO_INTEGER(QIDBUF(QNUM));
930 / * QUAD#_IN_GROUP=NVAL_OF_QID MOD 10;
931 / * QUAD_GROUP=NVAL_OF_QID/10;
932 / * DO CASE QUAD_GROUP; / * DECIDE ACCORDING TO THE GROUP OF QUAD
933 / * CALL DIR_BRNCHQUAD#_IN_GROUP); / * CASE 0
934 / * OUTPUT--NO INDIRECT BRANCH HAS BEEN IMPLEMENTED YET; / * CASE 1
935 / * CALL DECLARATION(QUAD#_IN_GROUP); / * CASE 2
936 / * CALL ARITH_OPIQUAD#_IN_GROUP); / * CASE 3
937 / * CALL SHIFT_OPIQUAD#_IN_GROUP); / * CASE 4
938 / * CALL LOGIC_OPIQUAD#_IN_GROUP); / * CASE 5
939 / * CALL MOVE_CONVQUAD#_IN_GROUP); / * CASE 6
940 / * CALL MISCQUAD#_IN_GROUP); / * CASE 7
941 / * END; / * OF CASE STATEMENT
942 / * END; / * OF IF THEN DO
943 / * ELSE SKIP_NEXT_QUAD=0;
944 / * END; / * OF DO QNUM=0
945 / * END DRIVER;
946 / *
947 / *
948 / *
949 / *
950 / *
951 / * QUAD_NUM# IS THE NUMBER OF QUADS TO BE READ IN.
952 / * THE PROCEDURE IS TO EXAMINE EACH ENTRY IN QIDBUF# TO FIND IF ITS VALUE
953 / * IS =62, THEN EXAMINE LEADING BYTE IN 2ND OPERAND(QOP2) AND IF IT IS =0,
954 / * THEN CALL PROCEDURE SYMBTAVL# TO GENERATE A VARIABLE SYMBOL, STORE INTO AN#
955 / * ARRAY INDEX_SYMB(INDEX#), INCREMENT THE INDEX# BY ONE.
956 / *
957 / * FIND_INDEX:=PROCEDURE(QUAD_NUM#);
958 / * DECLARE (QUAD_NUM#,I) FIXED, SYMBOL CHARACTER;
959 / * DO I = 0 TO QUAD_NUM#;
960 / * IF QIDBUF(I)=62, THEN
961 / * DO;
962 / * IF BYTE(QOP2(I),1)=BYTE('U') THEN
963 / * DO;
964 / * SYMBOL=SYMBTAVL(QOP2(I));
965 / * INDEX_SYMB(INDEX#)=SYMBOL;
966 / * INDEX#=INDEX#+1;
967 / * END; / * OF IF THEN DO
968 / * END; / * OF IF THEN DO
969 / * END; / * OF DO I=0
970 / * END FIND_INDEX;
971 / *
972 / *
973 / *
974 / * THE PROCEDURE IS TO READ IN AND ECHO-PRINT THE INPUT QUADS AS WELL STORE
975 / * THEM IN THE FOLLOWING FORMAT:
976 / * QUADNAME=COLUMN 1-4
977 / * QUADTYPE=COLUMN 5
978 / * CPT1 = COLUMN 7-17

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382 | /***** QUADS:PROCEDURE;
383 | INF QUADS:PROCEDURE;
384 | DEL=ARE QRECORD CHARACTER;
385 | /* READ, STORE AND ECHO PRINT QUADS, MAXIMUM 100 QUADS ARE STORED */
386 | OUTPUT=INPUT QUADS:;
387 | QUTPUT,QRECORD=INPUT; /* GET A QUAD */
388 | DO WHILE(LENGTH(QRECORD)>0) & (#OF_QUADS<=QRECFSIZE);
389 | QUADNAME(#OF_QUADS)=SUBSTR(QRECORD,1,4);
390 | QUADTYPE(#OF_QUADS)=SUBSTR(QRECORD,5,1);
391 | QOP1(#OF_QUADS)=SUBSTR(QRECORD,7,1);
392 | QOP2(#OF_QUADS)=SUBSTR(QRECORD,19,1);
393 | QOP3(#OF_QUADS)=SUBSTR(QRECORD,31,1);
394 | QIDRUF(#OF_QUADS)=SUBSTR(QRECORD,43,2);
395 | #OF_QUADS=#OF_QUADS+1;
396 | OUTPUT,QRECORD=INPUT; /* GET A NEW QUAD */
397 | END; /* OF DO WHILE */
398 | END INPUT_QUADS;
399 | /*****
400 | /*
401 | /*
402 | /* THE MAIN PROGRAM FIRST CALLS THE PROCEDURE 'INPUT_QUADS' TO READ IN
403 | /*AND ECHO-PRINT THE INPUT QUADS. THEN CALLS THE PROCEDURE 'FIND_INDEX' AND
404 | /*PROCEDURE 'DRIVER' TO PROCESS EACH QUAD AND CONVERT IT INTO VAX ASSEMBLY
405 | /*LANGUAGE.
406 | /*****
407 | CALL INPUT_QUADS; /* READ AND STORE MAXIMUM HUNDRED QUADS */
408 | /*
409 | /* PROCESS STORED QUADS
410 | CALL FIND_INDEX(#OF_QUADS);
411 | CALL DRIVER(#OF_QUADS);
412 | /*
413 | /* OUTPUT ASSEMBLY VERSION OF QUADS
414 | CALL OUTPUT_VASMIO,#OF_GVINS-1,0);
415 | CALL OUTPUT_VASMIDECL#,#BUFSIZE,#OF_GVINS);
416 | EOF

```

FILE CONTROL BLOCK 26000 13000 2 1 13000 1088 7008
 LOAD FILE WRITTEN.
 END OF COMPILATION SEPTEMBER 1, 1980. CLOCK TIME = 18:50:54.91.

1016 CARDS CONTAINING 421 STATEMENTS WERE COMPILED.
 NO ERRORS WERE DETECTED.

14388 BYTES OF PROGRAM, 3005 OF DATA, 3272 OF DESCRIPTORS, 729 OF STRINGS. TOTAL CORE REQUIREMENT 21094 BYTES.

SYMBOL TABLE DUMP

DEF_SYM	: FIXED	AT 1780(11),	DECLARED ON LINE 41 AND REFERENCED 5 TIMES.
DEF_GVINS	: FIXED	AT 1772(11),	DECLARED ON LINE 27 AND REFERENCED 39 TIMES.
DEF_QUADS	: FIXED	AT 1400(11),	DECLARED ON LINE 14 AND REFERENCED 11 TIMES.
AFT_INDX	: BIT(18)	AT 1783(11),	DECLARED ON LINE 40 AND REFERENCED 3 TIMES.
ALLOCATION	: LABEL	AT 8794(11),	DECLARED ON LINE 598 AND REFERENCED 4 TIMES.
PARAMETER 1	: CHARACTER	AT 2984(11),	DECLARED ON LINE 599 AND REFERENCED 1 TIMES.
PARAMETER 2	: CHARACTER	AT 2988(11),	DECLARED ON LINE 599 AND REFERENCED 2 TIMES.
ARITH_OP	: LABEL	AT 11698(11),	DECLARED ON LINE 804 AND REFERENCED 1 TIMES.
PARAMETER 1	: BIT(18)	AT 2776(11),	DECLARED ON LINE 805 AND REFERENCED 1 TIMES.
BLANK	: CHARACTER	PROCEDURE AT 2134(14),	DECLARED ON LINE 138 AND REFERENCED 3 TIMES.
PARAMETER 1	: CHARACTER	AT 2472(11),	DECLARED ON LINE 139 AND REFERENCED 3 TIMES.
PARAMETER 2	: FIXED	AT 1892(11),	DECLARED ON LINE 139 AND REFERENCED 2 TIMES.
CHOOB_BRTYP	: LABEL	AT 3882(11),	DECLARED ON LINE 332 AND REFERENCED 2 TIMES.
PARAMETER 1	: BIT(18)	AT 2044(11),	DECLARED ON LINE 333 AND REFERENCED 2 TIMES.
PARAMETER 2	: BIT(18)	AT 2045(11),	DECLARED ON LINE 333 AND REFERENCED 1 TIMES.
COMP_CHKBR	: LABEL	AT 5882(11),	DECLARED ON LINE 460 AND REFERENCED 6 TIMES.
PARAMETER 1	: BIT(18)	AT 2225(11),	DECLARED ON LINE 461 AND REFERENCED 2 TIMES.
CONV_DATA	: LABEL	AT 3258(11),	DECLARED ON LINE 264 AND REFERENCED 5 TIMES.
PARAMETER 1	: CHARACTER	AT 2544(11),	DECLARED ON LINE 265 AND REFERENCED 1 TIMES.
PARAMETER 2	: CHARACTER	AT 2548(11),	DECLARED ON LINE 255 AND REFERENCED 1 TIMES.
PARAMETER 3	: CHARACTER	AT 2552(11),	DECLARED ON LINE 265 AND REFERENCED 1 TIMES.
CONVERT_ID_INTEG	: LABEL	AT 2244(11),	DECLARED ON LINE 156 AND REFERENCED 4 TIMES.
PARAMETER 1	: CHARACTER	AT 2480(11),	DECLARED ON LINE 157 AND REFERENCED 3 TIMES.
CTYPE	: CHARACTER	AT 2312(11),	DECLARED ON LINE 35 AND REFERENCED 2 TIMES.
DECL#	: FIXED	AT 1776(11),	DECLARED ON LINE 29 AND REFERENCED 8 TIMES.
DECLARATION	: LABEL	AT 11814(11),	DECLARED ON LINE 826 AND REFERENCED 1 TIMES.
PARAMETER 1	: BIT(18)	AT 2796(11),	DECLARED ON LINE 827 AND REFERENCED 0 TIMES.
DIR_BRNCH	: LABEL	AT 12102(11),	DECLARED ON LINE 848 AND REFERENCED 1 TIMES.
PARAMETER 1	: BIT(18)	AT 2826(11),	DECLARED ON LINE 849 AND REFERENCED 1 TIMES.
DRIVER	: LABEL	AT 12892(11),	DECLARED ON LINE 922 AND REFERENCED 1 TIMES.
PARAMETER 1	: FIXED	AT 2908(11),	DECLARED ON LINE 923 AND REFERENCED 1 TIMES.
FBRDESO	: FIXED	AT 1404(11),	DECLARED ON LINE 15 AND REFERENCED 2 TIMES.
FBRDESO_IND	: BIT(18)	AT 1444(11),	DECLARED ON LINE 16 AND REFERENCED 5 TIMES.
FBRBL_GEN	: LABEL	AT 12262(11),	DECLARED ON LINE 879 AND REFERENCED 1 TIMES.
PARAMETER 1	: FIXED	AT 2852(11),	DECLARED ON LINE 880 AND REFERENCED 1 TIMES.
FIND_INDX	: LABEL	AT 13332(11),	DECLARED ON LINE 956 AND REFERENCED 1 TIMES.
PARAMETER 1	: FIXED	AT 2952(11),	DECLARED ON LINE 957 AND REFERENCED 1 TIMES.
FLAG#	: BIT(18)	AT 1781(11),	DECLARED ON LINE 38 AND REFERENCED 6 TIMES.
GEN_REG#	: CHARACTER	AT 2396(11),	DECLARED ON LINE 36 AND REFERENCED 6 TIMES.
GLARL	: CHARACTER	PROCEDURE AT 338(14),	DECLARED ON LINE 285 AND REFERENCED 3 TIMES.
PARAMETER 1	: CHARACTER	AT 2568(11),	DECLARED ON LINE 286 AND REFERENCED 3 TIMES.
IDENT_OPX	: LABEL	AT 2920(11),	DECLARED ON LINE 235 AND REFERENCED 14 TIMES.
PARAMETER 1	: BIT(18)	AT 1968(11),	DECLARED ON LINE 236 AND REFERENCED 2 TIMES.
IDENT_UTOPX	: LABEL	AT 2666(11),	DECLARED ON LINE 194 AND REFERENCED 1 TIMES.
PARAMETER 1	: BIT(18)	AT 1948(11),	DECLARED ON LINE 199 AND REFERENCED 1 TIMES.
INDX_REG	: CHARACTER	AT 2436(11),	DECLARED ON LINE 39 AND REFERENCED 5 TIMES.
INDX_SYMB	: CHARACTER	AT 2420(11),	DECLARED ON LINE 39 AND REFERENCED 2 TIMES.
INDX#	: BIT(18)	AT 1784(11),	DECLARED ON LINE 40 AND REFERENCED 5 TIMES.

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LAL4      : BIT(1)      AT 1793(11),      DECLARED ON LINE 37 AND REFERENCED 3 TIMES.
LOGIC_OP  : LABEL      AT 10712(14),      DECLARED ON LINE 742 AND REFERENCED 1 TIMES.
PARAMETER 1 : BIT(8)    AT 2668(11),      DECLARED ON LINE 743 AND REFERENCED 7 TIMES.
MISC      : LABEL      AT 10282(14),      DECLARED ON LINE 697 AND REFERENCED 1 TIMES.
PARAMETER 1 : FIXED     AT 2608(11),      DECLARED ON LINE 698 AND REFERENCED 1 TIMES.
MOVE_CONV : LABEL      AT 10608(14),      DECLARED ON LINE 730 AND REFERENCED 1 TIMES.
PARAMETER 1 : BIT(8)    AT 2648(11),      DECLARED ON LINE 731 AND REFERENCED 1 TIMES.
NAME      : CHARACTER AT 2228(13),        DECLARED ON LINE 35 AND REFERENCED 2 TIMES.
NVAL_OF_QID : BIT(8)   AT 1398(11),        DECLARED ON LINE 13 AND REFERENCED 6 TIMES.
QPD       : CHARACTER AT 2416(13),        DECLARED ON LINE 36 AND REFERENCED 29 TIMES.
OPXCT     : CHARACTER AT 2412(13),        DECLARED ON LINE 36 AND REFERENCED 14 TIMES.
OPICT     : CHARACTER AT 2400(13),        DECLARED ON LINE 36 AND REFERENCED 25 TIMES.
DP2CT     : CHARACTER AT 2404(13),        DECLARED ON LINE 36 AND REFERENCED 33 TIMES.
OP3CT     : CHARACTER AT 2408(13),        DECLARED ON LINE 36 AND REFERENCED 30 TIMES.
OUTPUT_VAS4 : LABEL    AT 12564(14),      DECLARED ON LINE 899 AND REFERENCED 2 TIMES.
PARAMETER 1 : FIXED     AT 2888(11),      DECLARED ON LINE 900 AND REFERENCED 1 TIMES.
PARAMETER 2 : FIXED     AT 2892(11),      DECLARED ON LINE 900 AND REFERENCED 1 TIMES.
PARAMETER 3 : FIXED     AT 2896(11),      DECLARED ON LINE 900 AND REFERENCED 3 TIMES.
PROC_ARITH : LABEL      AT 7088(14),      DECLARED ON LINE 506 AND REFERENCED 3 TIMES.
PARAMETER 1 : CHARACTER AT 2848(13),      DECLARED ON LINE 507 AND REFERENCED 2 TIMES.
PROC_BG    : LABEL      AT 9134(14),      DECLARED ON LINE 629 AND REFERENCED 1 TIMES.
PROC_BR    : LABEL      AT 10000(14),     DECLARED ON LINE 664 AND REFERENCED 1 TIMES.
PROC_INDX  : LABEL      AT 4558(14),      DECLARED ON LINE 368 AND REFERENCED 1 TIMES.
PROC_MOV   : LABEL      AT 5048(14),      DECLARED ON LINE 402 AND REFERENCED 1 TIMES.
PROC_UNST  : LABEL      AT 5700(14),      DECLARED ON LINE 434 AND REFERENCED 1 TIMES.
QBRFLG     : BIT(8)     AT 1340(11),      DECLARED ON LINE 7 AND REFERENCED 2 TIMES.
QIDBUF     : CHARACTER AT 1044(13),        DECLARED ON LINE 6 AND REFERENCED 10 TIMES.
QNUM       : FIXED      AT 1392(11),      DECLARED ON LINE 12 AND REFERENCED 65 TIMES.
QDP1       : CHARACTER AT 228(13),        DECLARED ON LINE 6 AND REFERENCED 14 TIMES.
QDP2       : CHARACTER AT 432(13),        DECLARED ON LINE 6 AND REFERENCED 11 TIMES.
QDP3       : CHARACTER AT 636(13),        DECLARED ON LINE 6 AND REFERENCED 6 TIMES.
QUAD_GROUP : BIT(8)     AT 1396(11),      DECLARED ON LINE 13 AND REFERENCED 2 TIMES.
QUAD#_IN_GROUP : BIT(8)  AT 1397(11),      DECLARED ON LINE 13 AND REFERENCED 8 TIMES.
QUADNAME   : CHARACTER AT 24(13),         DECLARED ON LINE 6 AND REFERENCED 1 TIMES.
QUADTYPE   : CHARACTER AT 840(13),        DECLARED ON LINE 6 AND REFERENCED 1 TIMES.
SEARCH_TYPE : CHARACTER PROCEDURE AT 1364(14), DECLARED ON LINE 66 AND REFERENCED 1 TIMES.
PARAMETER 1 : CHARACTER AT 2448(13),      DECLARED ON LINE 67 AND REFERENCED 1 TIMES.
SHIFT_OP   : LABEL      AT 11088(14),     DECLARED ON LINE 775 AND REFERENCED 1 TIMES.
PARAMETER 1 : BIT(8)    AT 2720(11),      DECLARED ON LINE 776 AND REFERENCED 0 TIMES.
SKIP_NEXT_QUAD : BIT(8)  AT 1445(11),      DECLARED ON LINE 17 AND REFERENCED 6 TIMES.
SRCH_FBRDESQ : LABEL     AT 10078(14),     DECLARED ON LINE 679 AND REFERENCED 1 TIMES.
PARAMETER 1 : FIXED     AT 2596(11),      DECLARED ON LINE 681 AND REFERENCED 1 TIMES.
SRCH_INDX  : CHARACTER PROCEDURE AT 2430(14), DECLARED ON LINE 175 AND REFERENCED 2 TIMES.
PARAMETER 1 : CHARACTER AT 2484(13),      DECLARED ON LINE 176 AND REFERENCED 1 TIMES.
PARAMETER 2 : BIT(8)    AT 1925(11),      DECLARED ON LINE 176 AND REFERENCED 2 TIMES.
SRCH_ONUM  : LABEL      AT 1478(14),      DECLARED ON LINE 83 AND REFERENCED 1 TIMES.
PARAMETER 1 : FIXED     AT 1844(11),      DECLARED ON LINE 84 AND REFERENCED 3 TIMES.
STOR_VAX_INS : LABEL     AT 1290(14),      DECLARED ON LINE 50 AND REFERENCED 27 TIMES.
PARAMETER 1 : CHARACTER AT 2440(13),      DECLARED ON LINE 51 AND REFERENCED 1 TIMES.
PARAMETER 2 : CHARACTER AT 2444(13),      DECLARED ON LINE 51 AND REFERENCED 1 TIMES.
PARAMETER 3 : FIXED     AT 1796(11),      DECLARED ON LINE 51 AND REFERENCED 1 TIMES.
PARAMETER 4 : FIXED     AT 1800(11),      DECLARED ON LINE 51 AND REFERENCED 4 TIMES.
SUBENT_ADDR : LABEL      AT 8648(14),      DECLARED ON LINE 576 AND REFERENCED 1 TIMES.
SVMBTAYL   : CHARACTER PROCEDURE AT 1732(14), DECLARED ON LINE 116 AND REFERENCED 15 TIMES.
PARAMETER 1 : CHARACTER AT 2452(13),      DECLARED ON LINE 117 AND REFERENCED 8 TIMES.
VLABEL_FLD : CHARACTER AT 1248(13),      DECLARED ON LINE 22 AND REFERENCED 9 TIMES.
VOPERAT    : CHARACTER AT 2220(13),      DECLARED ON LINE 28 AND REFERENCED 14 TIMES.
VOPERAT_FLD : CHARACTER AT 1572(13),      DECLARED ON LINE 22 AND REFERENCED 4 TIMES.
VOPRND     : CHARACTER AT 2224(13),      DECLARED ON LINE 28 AND REFERENCED 12 TIMES.
VOPRND_FLD : CHARACTER AT 1896(13),      DECLARED ON LINE 22 AND REFERENCED 4 TIMES.
VQNUM      : FIXED      AT 1448(11),      DECLARED ON LINE 23 AND REFERENCED 6 TIMES.

```

MACRO DEFINITIONS:

DIGIT LITERALLY: 0123456789
 DA_SIZE LITERALLY: 500
 DBUFSIZE LITERALLY: 50
 VBUFSIZE LITERALLY: 80
 MAX#_OF_FBR LITERALLY: 9
 MAX#_OF_SYMB LITERALLY: 20

IDCOMPARES = 42852
 SYMBOL_TABLE_SIZE = 143
 MACRO_DEFINITIONS = 6
 STACKING_DECISIONS = 18226
 SCAN = 4834
 EMITR = 548
 EMITRX = 3438
 FORCFACCUMULATOR = 1356
 ARITHMIT = 230
 GENSTORE = 243
 FIX8FW = 262
 FIXDATAWORD = 12
 FIXCHW = 435
 GETDATA = 0
 GETCODE = 3
 FINDADDRESS = 698
 SHORTCFIX = 429
 LONGCFIX = 6
 SHORTDFIX = 12
 LONGDFIX = 0
 FREE_STRING_AREA = 111222

REGISTER VALUES (RELATIVE TO R11):

R4 = 0
 R5 = 0
 R6 = 0
 R7 = 0
 R8 = 0
 R9 = 0
 R10 = 0
 R11 = 0
 R12 = 0
 R13 = 3000

INSTRUCTION FREQUENCIES:

BALR 28
 BCTR 3
 BCR 56
 LPR 1
 LTR 9
 LCR 1
 NR 19
 OR 12
 XR 63
 LR 180
 CR 7
 AR 27

LA	256
STC	81
IC	97
EX	62
RAL	201
BC	408
LH	6
ST	593
N	33
M	18
D	1058
L	66
C	58
A	31
S	2
M	5
D	2
AL	2
SL	2
SRL	65
SLL	94
SRA	60
SRDA	5
STH	28
TM	3
DI	1
LH	29

TOTAL TIME IN COMPILER 0:1:49.22.
 SET UP TIME 0:0:7.21.
 ACTUAL COMPILATION TIME 0:1:34.99.
 POST-COMPILATION TIME 0:0:7.02.
 COMPILATION RATE: 641 CARDS PER MINUTE.

Appendix A2
Quadruple To VAX 11/780
Microcode Translator
with Example

TODAY 1. SEPTEMBER 2, 1980. CLOCK TIME = 10:23:30.07.

Line	Code	Address
1	1286	1286
2	1286	1286
3	1286	1286
4	1286	1286
5	1286	1286
6	1286	1286
7	1286	1286
8	1286	1286
9	1286	1286
10	1286	1286
11	1286	1286
12	1286	1286
13	1286	1286
14	1286	1286
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92	1286	1286
93	1286	1286
94	1286	1286
95	1286	1286
96	1286	1286
97	1286	1286
98	1286	1286
99	1286	1286
100	1286	1286


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123 | LABEL_FLD_INDX(QNUM)=FOP_LINE;
124 | IF (SUBSTR(OP1,0,1)=0) & (SUBSTR(OP3,0,1)=0) THEN
125 | DO;
126 | MOP3=FIND_REGM(OP3);
127 | BLIN_CONST=IDENT_CONST(SUBSTR(OP1,1));
128 | IF BLIN_CONST=1 THEN
129 | DO;
130 | IF OP1=0 THEN MICRO_OPRT_FLD(OF_LINE)=R(,1)MOP3;
131 | ELSE MICRO_OPRT_FLD(OF_LINE)=R(,1)MOP3;
132 | CALL COMENT_LINE;
133 | END; /* OF IF THEN DO */
134 | ELSE OUTPUT=NON-BLIN-CONSTANT NOT IMPLEMENTED YET;
135 | END; /* OF IF THEN DO */
136 | IF (SUBSTR(OP1,0,1)=0) & (SUBSTR(OP3,0,1)=0) THEN
137 | DO;
138 | MOP1=FIND_REGM(OP1);
139 | MOP3=FIND_REGM(OP3);
140 | MICRO_OPRT_FLD(OF_LINE)=LAB_RL(1)MOP1;
141 | CALL COMENT_LINE;
142 | MICRO_OPRT_FLD(OF_LINE)=R(,1)MOP3;
143 | CALL COMENT_LINE;
144 | END; /* OF IF THEN DO */
145 | ELSE OUTPUT=THIS TYPE OF MOVE HAS NOT BEEN IMPLEMENTED YET;
146 | END; /* OF ELSE DO */
147 | END PROC_MOV;
148 | /*****
149 | /***** PROCEDURE PROC_INDX
150 | /*****
151 | /*****
152 | /***** PROC_INDX: PROCEDURE
153 | /*****
154 | /***** PROC_INDX: PROCEDURE
155 | /*****
156 | /***** PROC_INDX: PROCEDURE
157 | /*****
158 | /***** PROCEDURE MOV_CONV
159 | /*****
160 | /***** MOV_CONV: PROCEDURE(QINGRP);
161 | /***** DECLARE QINGRP BIT(8);
162 | /***** DO CASE QINGRP;
163 | /***** CALL PROC_MOV;
164 | /***** OUTPUT=QUAD NUMBER IS 61. NOT IMPLEMENTED YET;
165 | /***** CALL PROC_INDX;
166 | /***** END; /* OF DO CASE */
167 | /***** END MOV_CONV;
168 | /*****
169 | /***** PROCEDURE ARITH_OP
170 | /*****
171 | /***** ARITH_OP: PROCEDURE(I);
172 | /***** DECLARE I BIT(8); (OP1,OP2,OP3,MOP1,MOP2,MOP3) CHARACTER,
173 | /***** BLIN_CONST BIT(1);
174 | /***** OP1=SYMBTAYL(QUADOPD1(QNUM));
175 | /***** OP2=SYMBTAYL(QUADOPD2(QNUM));
176 | /***** OP3=SYMBTAYL(QUADOPD3(QNUM));
177 | /***** LABEL_FLD_INDX(QNUM)=FOP_LINE;
178 | /***** IF 1=0 THEN
179 | /***** IF (SUBSTR(OP1,0,1)=0) & (SUBSTR(OP2,0,1)=0) & (SUBSTR(OP3,0,1)=0) THEN
180 | /***** DO;
181 | /***** MOP1=FIND_REGM(OP1);
182 | /***** MOP2=FIND_REGM(OP2);
183 | /***** MOP3=FIND_REGM(OP3);
184 | /***** MICRO_OPRT_FLD(OF_LINE)=Q_RL(1)MOP1;
185 | /***** CALL COMENT_LINE;
186 | /*****

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C13 - 16777215.

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2484 PROC_MOV
2498 PROC_MOV
2604 PROC_MOV
2612 PROC_MOV
2628 PROC_MOV
2654 PROC_MOV
2676 PROC_MOV
2688 PROC_MOV
2734 PROC_MOV
2766 PROC_MOV
2826 PROC_MOV
2892 PROC_MOV
2896 PROC_MOV
2920 PROC_MOV
2920 PROC_MOV
2924 PROC_MOV
3030 PROC_MOV
3038 PROC_MOV
3054 PROC_MOV
3070 PROC_MOV
3134 PROC_MOV
3138 PROC_MOV
3202 PROC_MOV
3206 PROC_MOV
3206 PROC_MOV
3230 PROC_MOV
3230 PROC_MOV
3236 PROC_MOV
3236
3236
3236
3236 PROC_INDX
3264 PROC_INDX
3270
3270
3270
3270 MOV_CONV
3278 MOV_CONV
3300 MOV_CONV
3304 MOV_CONV CASE 0.
3328 MOV_CONV CASE 1.
3336 MOV_CONV CASE 2.
3340 MOV_CONV
3346
3346
3346
3346 ARITH_OP
3354 ARITH_OP
3354 ARITH_OP
3380 ARITH_OP
3406 ARITH_OP
3432 ARITH_OP
3446 ARITH_OP
3468 ARITH_OP
3566 ARITH_OP
3622 ARITH_OP
3630 ARITH_OP
3646 ARITH_OP
3662 ARITH_OP
3678 ARITH_OP
3742 ARITH_OP
3746 ARITH_OP

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199 | MICRO_OPRT_FLD(OF_LINEL)=K(.'||MOP3||'.)_ALU, ALU_LA+Q;';
200 | CALL COMENT_LINEL;
201 | END; /* IF THEN DO */
202 | ELSE DO;
203 | IF (SUBSTR(OP1,0,1))=K(.'||SUBSTR(OP3,0,1))=U') THEN
204 | DO;
205 | MOP3=FINO_REG#(MOP3);
206 | BLIN_CONST=IDENT_CONST(SUBSTR(OP1,1));
207 | IF BLIN_CONST=1 THEN
208 | DO;
209 | MICRO_OPRT_FLD(OF_LINEL)=LAB_R(.'||MOP3||'.);';
210 | CALL COMENT_LINEL;
211 | MICRO_OPRT_FLD(OF_LINEL)=ALU_LA+K(.'||SUBSTR(OP1,1)||'.);';
212 | #OF_LINEL=#OF_LINEL+1;
213 | MICRO_OPRT_FLD(OF_LINEL)=R(.'||MOP3||'.)_ALU;';
214 | CALL COMENT_LINEL;
215 | END; /* OF IF THEN DO */
216 | ELSE OUTPUT=NON-BLIN-CONSTANT HAS NOT IMPLEMENTED YET;
217 | END; /* OF IF THEN DO */
218 | ELSE OUTPUT=SUCH TYPE OF ADD QUAD NOT IMPLEMENTED YET;
219 | END; /* OF ELSE DO */
220 | IF I=0 THEN
221 | OUTPUT=NOT IMPLEMENTED YET;
222 | END ARITH_OP;
223 | /*****
224 | /*
225 | PROCEDURE GLABL
226 | GLABL: PROCEDURE(OPX);
227 | DECLARE VOPD BIT(8); OPX CHARACTER;
228 | VOPD=CONVERT_TO_INTEG(OPX);
229 | IF VOPD<QNUN THEN
230 | DO;
231 | IF SUBSTR(MICRO_LABL_FLD(OF_LINEL),0,5)='LABL-' THEN
232 | MICRO_OPRT_FLD(OF_LINEL)=J(.'||MICRO_LABL_FLD(LABL_FLD_INDX(VOPD))
233 | ||'.);
234 | ELSE DO;
235 | MICRO_OPRT_FLD(OF_LINEL)=J/LABL-'||SUBSTR(ALPHA,IN#+1)||'.;';
236 | MICRO_LABL_FLD(OF_LINEL)=LABL-'||SUBSTR(ALPHA,IN#+1)
237 | ||'.;';
238 | IN#=IN#+1;
239 | END; /* OF ELSE DO */
240 | ELSE DO;
241 | QBRFLG(VOPD)=1;
242 | FBRESQ(INDEX)=VOPD;
243 | MICRO_OPRT_FLD(OF_LINEL)=J/LBLF-'||SUBSTR(ALPHA,INDEX)||'.;';
244 | INDEX=INDEX+1;
245 | END; /* OF ELSE DO */
246 | CALL COMENT_LINEL;
247 | END GLABL;
248 | /*****
249 | /*
250 | PROCEDURE PROC_BR
251 | PROC_BR: PROCEDURE;
252 | DECLARE OP1 CHARACTER;
253 | OP1=SYMBTAYLIQUADDPD(IONUM);
254 | LARL_FLD_INDX(IONUM)=#OF_LINEL;
255 | CALL GLABL(OP1);
256 | END PROC_BR;
257 | /*****
258 | /*
259 | PROCEDURE PROC_BG
260 | PROC_BG: PROCEDURE;
261 | DECLARE (OP1,OP2,OP3,MOP2,MOP3) CHARACTER, VOPD BIT(8);

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C14 = 67108864.

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255 | UP=SYTIME*1000/(QUAD*OP3)(QNUM);
256 | MOP2=FIND_REF#(OP2);
257 | MOP3=FIND_NEG#(OP3);
258 | LABEL_FLD_INDX(QNUM)=#OF_LINE;
259 | MICRO_OPRT_FLD#(OF_LINE)=Q_R#(MOP2|'.');
260 | CALL COMENT_LINE;
261 | MICRO_OPRT_FLD#(OF_LINE)=VALU_LA-Q';
262 | MICRO_OPRT_FLD#(OF_LINE+1)=LAB_R#(MOP3|'.');
263 | MICRO_OPRT_FLD#(OF_LINE+2)=CLK.UBCC';
264 | #OF_LINE=#OF_LINE+2;
265 | CALL COMENT_LINE;
266 | MICRO_OPRT_FLD#(OF_LINE)=ALU?';
267 | #OF_LINE=#OF_LINE+1;
268 | MICRO_LABEL_FLD#(OF_LINE)=1110';
269 | MICRO_OPRT_FLD#(OF_LINE)=;
270 | #OF_LINE=#OF_LINE+1;
271 | CALL GLABL(OP1);
272 | END PROC_BG;
273 | /*****
274 | /* PROCEDURE DIR_BRNCH
275 | /*****
276 | DIR_BRNCH:PROCEDURE(QINGRP);
277 | DECLARE QINGRP BIT(8);
278 | DO CASE QINGRP;
279 | CALL PROC_BR;
280 | OUTPUT=NO PROC_BZ YET';
281 | OUTPUT=NO PROC_BP YET';
282 | OUTPUT=NO PROC_BN YET';
283 | CALL PROC_BG;
284 | END; /* OF DO CASE */
285 | END DIR_BRNCH;
286 | /*****
287 | /* PROCEDURE PROC_UNST
288 | /*****
289 | PROC_UNST:PROCEDURE;
290 | LABEL_FLD_INDX(QNUM)=#OF_LINE;
291 | IF IDENT_QNAME(QUADNAME(QNUM+1))=75 THEN
292 | DO;
293 | SKIP_NEXT_QUAD=1;
294 | MICRO_OPRT_FLD#(OF_LINE)=PC_PC+1, CLR_IB.OPC';
295 | MICRO_OPRT_FLD#(OF_LINE+1)=J/J62';
296 | #OF_LINE=#OF_LINE+1;
297 | CALL COMENT_LINE;
298 | END; /* OF IF THEN DO */
299 | ELSE OUTPUT=NOT IMPLEMENTED YET';
300 | END PROC_UNST;
301 | /*****
302 | /* PROCEDURE PROC_RETN
303 | /*****
304 | PROC_RETN:PROCEDURE;
305 | OUTPUT=NOT IMPLEMENTED YET';
306 | END PROC_RETN;
307 | /*****
308 | /* PROCEDURE MISC
309 | /*****
310 | MISC:PROCEDURE(QINGRP);
311 | DECLARE QINGRP FIXED;
312 | ON CASE QINGRP;
313 | OUTPUT=NOT IMPLEMENTED YET';
314 | OUTPUT=NOT IMPLEMENTED YET';
315 | OUTPUT=NOT IMPLEMENTED YET';
316 | OUTPUT=NOT IMPLEMENTED YET';
317 | CALL PROC_RETN;
318 |
319 |
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453 | 17) DRIVER;
454 | /*****
455 | *****
456 | /
457 | OUTPUT_MICRO:PROCEDURE;
458 |   DECLARE (S1,S2) CHARACTER, N FIXED;
459 |   DO N=0 TO #OF_LINE;
460 |     S1=BLANK(MICRO_LABL_FLDIN),13);
461 |     S2=BLANK(MICRO_OPMT_FLDIN),13);
462 |     OUTPUT=
463 |       '11S111S2';
464 |   END; /* OF DO STATEMENT */
465 | END OUTPUT_MICRO;
466 | /*****
467 | /*
468 |   ***MAIN PROGRAM***
469 | /*****
470 | ALPHA='ABCDEFGHIJKLMNQRSTUVMXYZ';
471 | DIGIT='0123456789';
472 | CALL INPUT_QUADS;
473 | CALL DRIVER(#OF_QUADS);
474 | OUTPUT(1)=1;
475 | CALL OUTPUT_MICRO;
476 | EOF EOF EOF

```

* FILE CONTROL BLOCK 13000 13000 1 1 13000 8244 5968
 * LOAD FILE WRITTEN.
 END OF COMPILATION SEPTEMBER 2, 1980. CLOCK TIME = 10:25:46.47.
 474 CARDS CONTAINING 260 STATEMENTS WERE COMPILED.
 NO ERRORS WERE DETECTED.
 8242 BYTES OF PROGRAM, 2133 OF DATA, 2356 OF DESCRIPTORS, 1476 OF STRINGS. TOTAL CORE REQUIREMENT 14207 BYTES.

SYMBOL TABLE DUMP

#OF_LINE	: FIXED	AT 1340(111),	DECLARED ON LINE 7 AND REFERENCED 57 TIMES.
#OF_QUADS	: FIXED	AT 1352(111),	DECLARED ON LINE 8 AND REFERENCED 8 TIMES.
ALPHA	: CHARACTER	AT 1306(113),	DECLARED ON LINE 15 AND REFERENCED 5 TIMES.
ARITH_OP	: LABEL	AT 3350(114),	DECLARED ON LINE 171 AND REFERENCED 1 TIMES.
PARAMETER 1	: BIT(18)	AT 1676(111),	DECLARED ON LINE 172 AND REFERENCED 2 TIMES.
BLANK	: CHARACTER PROCEDURE	AT 7010(114),	DECLARED ON LINE 405 AND REFERENCED 2 TIMES.
PARAMETER 1	: CHARACTER	AT 2312(113),	DECLARED ON LINE 406 AND REFERENCED 3 TIMES.
PARAMETER 2	: FIXED	AT 2040(111),	DECLARED ON LINE 406 AND REFERENCED 2 TIMES.
CONST_ARRAY	: LABEL	AT 2062(114),	DECLARED ON LINE 83 AND REFERENCED 12 TIMES.
CONVERT_TO_INTG	: CHARACTER	AT 1624(113),	DECLARED ON LINE 29 AND REFERENCED 1 TIMES.
PARAMETER 1	: LABEL	AT 2116(114),	DECLARED ON LINE 91 AND REFERENCED 1 TIMES.
DECLARATION	: CHARACTER	AT 1888(113),	DECLARED ON LINE 92 AND REFERENCED 2 TIMES.
PARAMETER 1	: LABEL	AT 6404(114),	DECLARED ON LINE 361 AND REFERENCED 1 TIMES.
DIGIT	: BIT(18)	AT 2010(111),	DECLARED ON LINE 362 AND REFERENCED 0 TIMES.
DIR_BRANCH	: CHARACTER	AT 1308(113),	DECLARED ON LINE 15 AND REFERENCED 2 TIMES.
PARAMETER 1	: LABEL	AT 5398(114),	DECLARED ON LINE 276 AND REFERENCED 1 TIMES.
DRIVER	: BIT(18)	AT 1892(111),	DECLARED ON LINE 277 AND REFERENCED 1 TIMES.
PARAMETER 1	: LABEL	AT 7534(114),	DECLARED ON LINE 431 AND REFERENCED 1 TIMES.
FBRDESO	: BIT(18)	AT 2076(111),	DECLARED ON LINE 432 AND REFERENCED 1 TIMES.
FBRLABL_GEN	: BIT(18)	AT 1302(111),	DECLARED ON LINE 11 AND REFERENCED 2 TIMES.
PARAMETER 1	: LABEL	AT 5996(114),	DECLARED ON LINE 326 AND REFERENCED 1 TIMES.
FIND_REC#	: BIT(18)	AT 1972(111),	DECLARED ON LINE 327 AND REFERENCED 1 TIMES.
PARAMETER 1	: CHARACTER PROCEDURE	AT 2240(114),	DECLARED ON LINE 102 AND REFERENCED 9 TIMES.
GLABL	: CHARACTER	AT 1896(113),	DECLARED ON LINE 103 AND REFERENCED 1 TIMES.
PARAMETER 1	: LABEL	AT 4390(114),	DECLARED ON LINE 216 AND REFERENCED 2 TIMES.
IDENT_CONST	: CHARACTER	AT 2092(113),	DECLARED ON LINE 217 AND REFERENCED 1 TIMES.
PARAMETER 1	: LABEL	AT 1494(114),	DECLARED ON LINE 52 AND REFERENCED 2 TIMES.
IDENT_QNAME	: CHARACTER	AT 1860(113),	DECLARED ON LINE 53 AND REFERENCED 1 TIMES.
PARAMETER 1	: LABEL	AT 1290(114),	DECLARED ON LINE 38 AND REFERENCED 4 TIMES.
IN#	: CHARACTER	AT 1852(113),	DECLARED ON LINE 39 AND REFERENCED 1 TIMES.
INDO#	: FIXED	AT 1344(111),	DECLARED ON LINE 7 AND REFERENCED 4 TIMES.
INDX	: BIT(18)	AT 1436(111),	DECLARED ON LINE 13 AND REFERENCED 5 TIMES.
INPUT_QUADS	: FIXED	AT 1348(111),	DECLARED ON LINE 8 AND REFERENCED 5 TIMES.
LABL_FLD_IND#	: LABEL	AT 7136(114),	DECLARED ON LINE 414 AND REFERENCED 1 TIMES.
LOGIC_OP	: BIT(18)	AT 1358(111),	DECLARED ON LINE 10 AND REFERENCED 8 TIMES.
PARAMETER 1	: LABEL	AT 6366(114),	DECLARED ON LINE 354 AND REFERENCED 0 TIMES.
MEM_LABL_GEN	: BIT(18)	AT 2000(111),	DECLARED ON LINE 355 AND REFERENCED 0 TIMES.
MICRO_LABL_FLD	: LABEL	AT 6290(114),	DECLARED ON LINE 341 AND REFERENCED 1 TIMES.
MISC	: CHARACTER	AT 568(113),	DECLARED ON LINE 5 AND REFERENCED 9 TIMES.
PARAMETER 1	: LABEL	AT 852(113),	DECLARED ON LINE 5 AND REFERENCED 27 TIMES.
MUV_CONV	: LABEL	AT 5754(114),	DECLARED ON LINE 310 AND REFERENCED 1 TIMES.
PARAMETER 1	: FIXED	AT 1932(111),	DECLARED ON LINE 311 AND REFERENCED 1 TIMES.
NVAL_OF_QID	: LABEL	AT 3274(114),	DECLARED ON LINE 160 AND REFERENCED 1 TIMES.
OPNI	: BIT(18)	AT 1656(111),	DECLARED ON LINE 161 AND REFERENCED 1 TIMES.
OUTPUT_MICRO	: BIT(18)	AT 1357(111),	DECLARED ON LINE 9 AND REFERENCED 8 TIMES.
PRIC_1G	: CHARACTER	AT 1136(113),	DECLARED ON LINE 6 AND REFERENCED 2 TIMES.
	: LABEL	AT 7976(114),	DECLARED ON LINE 457 AND REFERENCED 1 TIMES.
	: LABEL	AT 4990(114),	DECLARED ON LINE 251 AND REFERENCED 1 TIMES.

```

PRUC_MIV
PRUC_RFTV
PRUC_UN5
QBKFLG
QNUY
QOPND
QUAD_TAB
QUADNAME
QUADUPD1
QUADUPD2
QUADUPD3
SHIFT_OP
PARAMETER 1
SKIP_NEXT_QUAD
SYMBTAYL
PARAMETER 1

: LABEL
: LABEL
: LABEL
: BIT(8)
: BIT(8)
: CHARACTER
: CHARACTER
: CHARACTER
: CHARACTER
: CHARACTER
: CHARACTER
: LABEL
: BIT(8)
: BIT(8)
: CHARACTER PROCEDURE AT
: CHARACTER AT

AT 2424(14),
AT 5716(14),
AT 5558(14),
AT 1402(11),
AT 1356(11),
AT 1220(13),
AT 1312(13),
AT 2411(3),
AT 1601(3),
AT 2961(3),
AT 4321(3),
AT 6328(14),
AT 1992(11),
AT 1437(11),
1660(14),
DECLARED ON LINE 66 AND REFERENCED 8 TIMES.

DECLARED ON LINE 119 AND REFERENCED 1 TIMES.
DECLARED ON LINE 304 AND REFERENCED 1 TIMES.
DECLARED ON LINE 289 AND REFERENCED 1 TIMES.
DECLARED ON LINE 12 AND REFERENCED 2 TIMES.
DECLARED ON LINE 9 AND REFERENCED 23 TIMES.
DECLARED ON LINE 6 AND REFERENCED 2 TIMES.
DECLARED ON LINE 20 AND REFERENCED 1 TIMES.
DECLARED ON LINE 4 AND REFERENCED 5 TIMES.
DECLARED ON LINE 4 AND REFERENCED 6 TIMES.
DECLARED ON LINE 4 AND REFERENCED 3 TIMES.
DECLARED ON LINE 4 AND REFERENCED 4 TIMES.
DECLARED ON LINE 347 AND REFERENCED 1 TIMES.
DECLARED ON LINE 348 AND REFERENCED 0 TIMES.
DECLARED ON LINE 14 AND REFERENCED 4 TIMES.
DECLARED ON LINE 65 AND REFERENCED 10 TIMES.
DECLARED ON LINE 66 AND REFERENCED 8 TIMES.

```


MACRO DEFINITIONS:

DM_SIZE LITERALLY: 500

IDCOMPARES = 16966
 SYMBOL TABLE SIZE = 99
 MACRO DEFINITIONS = 1
 STACKING DECISIONS = 11886
 SCAN = 3316
 EMITR = 361
 ENITR = 1977
 FORCEACCUMULATOR = 778
 ARITHMIT = 133
 GENSTORE = 188
 FIXBFW = 149
 FIXDATAWORD = 12
 FIXCHW = 209
 GETDATA = 0
 GETCODE = 0
 FINDADDRESS = 472
 SHORTCFIX = 209
 LONGCFIX = 0
 SHORTDFIX = 12
 LONGDFIX = 0
 FREE STRING AREA = 11122

REGISTER VALUES (RELATIVE TO R11):

R4 = 0
 R5 = 0
 R6 = 0
 R7 = 0
 R8 = 0
 R9 = 0
 R10 = 0
 R11 = 0
 R12 = 0
 R13 = 2128

INSTRUCTION FREQUENCIES:

BALR	36
BCTR	3
BCR	40
LPR	1
LTR	8
NR	12
OR	4
XR	17
LR	53
CR	7
AR	22
SR	157
DR	1
STH	3
LA	156
STC	56
IC	99

BC	224
LH	3
ST	18
N	23
O	529
L	48
C	42
A	19
S	1
M	5
D	2
AL	4
SL	22
SRL	73
SLL	17
SRA	5
SROA	36
STM	1
TM	1
DI	1
LM	37

TOTAL TIME IN COMPILER 0:2:30.53.
 SET UP TIME 0:0:14.65.
 ACTUAL COMPILATION TIME 0:1:44.17.
 POST-COMPILATION TIME 0:0:31.71.
 COMPILATION RATES 273 CARDS PER MINUTE.

INPUT QUANTITY	ADDRESS	DATA	OPERATION	ADDRESS	DATA
0	ADDR	U000000010		U000000000	
1	ADDR	U000000011		000000002	
2	BYTE	U000000012		000000004	
3	ADDR	U000000013		000000006	
4	BYTE	U000000014		000000008	
5	ADDR	U000000015		000000010	
6	BYTE	U000000016		000000012	
7	ADDR	U000000017		U000000012	
8	BYTE	U000000018		U000000013	
9	ADDR	U000000019		U000000014	
10	BYTE	U000000020		U000000015	
11	ADDR	U000000021		U000000016	
12	MOV	U000000022		U000000017	
13	MOV	U000000023		U000000018	
14	MOV	U000000024		U000000019	
15	MOV	U000000025		U000000020	
16	MOV	U000000026		U000000021	
17	MOV	U000000027		U000000022	
18	MOV	U000000028		U000000023	
19	MOV	U000000029		U000000024	
20	ADD	U000000030		U000000025	
21	ADD	U000000031		U000000026	
22	ADD	U000000032		U000000027	
23	BR	U000000033		U000000028	
24	UNST	U000000034		U000000029	
25	RETN	U000000035		U000000030	

```

      .TOC '
      .REGION /1600,17FF

      INPUT
      R0 -- U11
      R1 -- U12
      R2 -- U13
      R3 -- U14
      R4 -- U15
      R5 -- U16

      R1.R1.K1..ZERO.);
      R1.R2.K1..1.);
      R1.R3.K1..10.);
      R1.R4.K1..1.);
      Q_R1.R4.);
      ALU_LA-Q,
      LAB_R1.R3.);
      CLK.UBCC;
      ALU?;
      J/LBLF-A;
      LAB_R1.R1.);
      R1.R0.LA;
      LAB_R1.R2.);
      R1.R1.LA;
      Q_R1.R0.);
      LAB_R1.R1.);
      R1.R5.ALU, ALU_LA+Q;
      LAB_R1.R5.);
      R1.R2.LA;
      LAB_R1.R4.);
      ALU_LA+K1..1.);
      R1.R4.ALU;
      J/LABL-A;
      PC_PC+1, CLR.BB.DPC,
      J/062;

```

LABL-A:

-1110

LBLF-A:

APPENDIX B

"USER" MICROPROGRAMMING MANUAL FOR THE DEC VAX 11/780

Teh-Hsin Yang

CONTENTS

- 1) Basic Architecture Features of VAX 11/780
- 2) MICRO2 - Microprogramming Assembler
- 3) How to load and execute a microprogram.
- 4) Using Control Command to debug the User Microprogram.

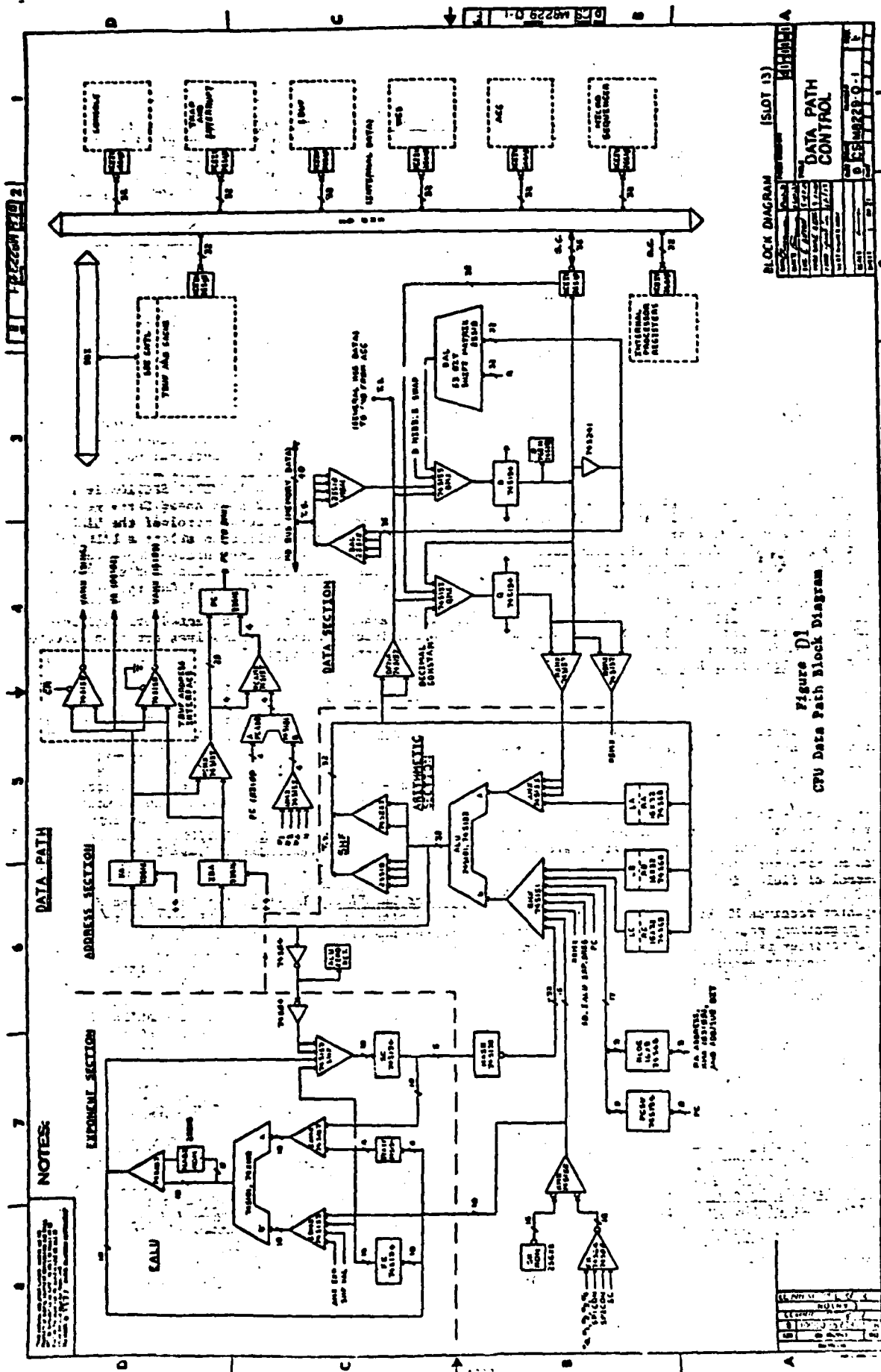
1) Basic Architecture Features of VAX 11/780

The VAX 11/780 is a general purpose microprogrammed computer. It features a 32 bit word, virtual sotrage which provides addressing of 2⁸ Bytes, an 8K cache storage unit, a 200 NS basic CPU cycle, and a powerful instruction set. This system includes 1024 words(96 bits) of "user" microprogrammable control store. Support software for microprogramming includes an assembler and debugger which permits the user to design their own microcode. It has been demonstrated that an algorithm expressed directly in microcode will execute faster than routines programmed in assembly or a high level language (HLL). Before describing this procedure for preparing microprograms for the VAX 11/780, a brief overview of the architecture of the CPU will be given. Special attention will be given to those parts which most profoundly affect the preparation of microprograms. Figure D1, which is a block diagram of the VAX 11/780 CPU, will support the ensuing discussion.

The VAX 11/780 CPU has two sets of sixteen 32 bit general purpose registers. A number of these registers have preassigned functions (R₁₂ = Argument list pointer, R₁₃ = Stack frame pointer, R₁₄ = Stack pointer, R₁₅ = PC. Registers R₀ thru R₇ are available to programmers. The output of the A registers passes through latch LA to the A side of the ALU while the output of the B registers passes through latch LB to the B side of the ALU. An additional set of 16 working 32 Bit Registers, RC, output thru an LC latch to the left side of the ALU. The RC registers are only available at the microcode level.

Two other 32 bit registers are named D and Q. They can be gated to either side of the ALU. The content of D register can be delivered to the Q Register directly without passing through the ALU. A rotation unit accepts the 64 bits from the Q and D registers and rotates it by the amount specified by a user instruction and deposits 32 bits of the shifted result back in the D register. The D register also acts as the memory data register and data read from and into storage must pass through this register.

The memory address register, VA, can be loaded from ALU or can be incremented by 4 which advances the address by one word (32 bits). There



is an auxiliary 10-bit exponent ALU (EALU) for handling floating point exponent computations. Its data path contains a register named SC which is used for shift operations and masking the data entering the left side of the ALU. Another feature of the VAX CPU is the constant generator. A ROM, called SK, provides 64 16 bit constants available to the left side of ALU.

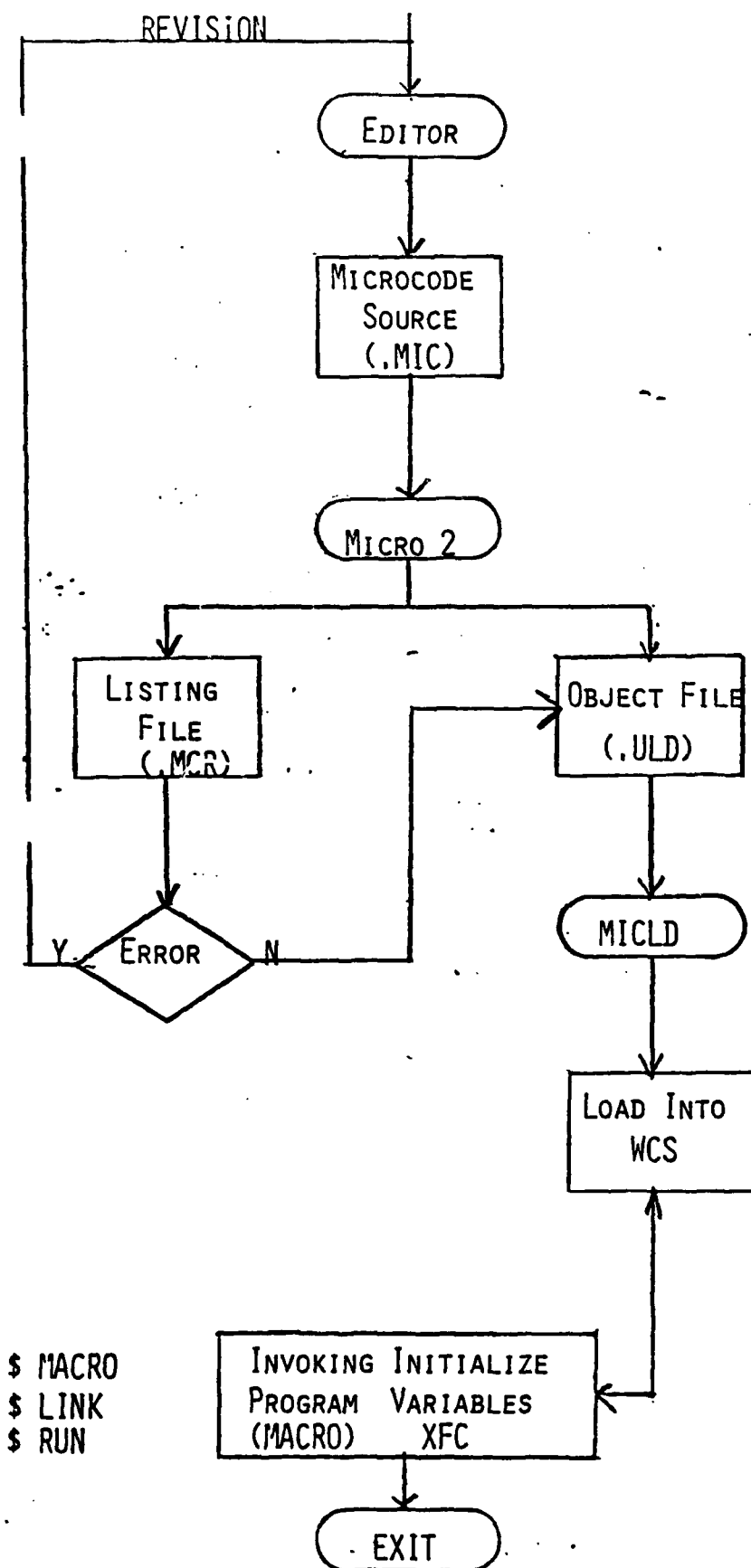
The VAX machine is controlled by a horizontal micro control word which is 96 bits wide and divided into 30 control fields. This represents a horizontal control word format and presents a complicated microprogram design problem. Many operations may be carried out in parallel. A detailed description of the micro control word is not given here since it is described in other manuals. But it will be useful to give a brief overview of branch micro-operations for each control word. Thirteen bits are used to form the address of next micro instruction. These can be assigned directly by the microprogram which corresponds to an unconditional branch at the microcode level. When a conditional branch is required, other micro control words are involved in establishing the branch conditions required. The BEN (Branch Enable) micro control field contains 5 bits which are used to specify twenty-six branch conditions. From this control field it is possible to select different program status words (PSWs), including the N, Z, V, C and other flags as Branch conditions. These conditions are ORed with the low-order bits of the micro address field (JMP) to form the address of the successor microword. In order to make a conditional branch occur, it is necessary to make sure the potential branch address has certain bits equal to zero so that the OR operation produces the appropriate branch address. The Micro-2 Assembler, to be described later, has the ability to make appropriate bits of a branch address equal to zero to satisfy the OR requirements.

2) Micro 2 - Microprogram Assembler

The process of writing, loading, and executing a microprogram in the VAX 11/780 "User" control storage area is described here. Figure D2 is a Flowchart which shows these steps. The first step in microprogramming the VAX 11/780 is generation of the microcode source load module. To do this, use is made of the VAX SOS Editor system which is initiated thru use of the edit command. The individual microprogram statements are entered along with comments as shown by example in Figure D3. While not required, certain formatting procedures are recommended to improve readability of this microcode. The formatting procedures are:

MICROCODE GENERATION PROTOCOLS

1. Precede Micro instruction by any general comments
2. If Micro instruction has explicit address--give that address at the left margin--put no info on that line.
3. If Micro instruction has a label--give label at left margin and put no other information on that line.
4. Include as many Micro instruction--parts separated by commas as will fit in columns starting at the second tab (col 17) and going to column 38.
5. Place line specific comments starting at 5th tab Col 41.



COMMAND

\$EDIT FILE NAME .MIC

\$MICRO 2 FILE NAME

\$MICLD FILE NAME

FIGURE D2 GENERATION
OF MICROCODE
FOR VAX 11/780

```

TYPE BUBBLE.MIC:8
.TITLE 'BUBBLE SORT'
.TOC 'ATTACHED MACRO DEFINITIONS'
ALU_Q+LB-1 'RAMX/Q,AMX/RAMX,BMX/LB,ALU/A+B'
.REGION /1400,17FF

; INPUTS
; ASSUMPTION
; R1-I
; R2-J
; R3-K
; R4-TEMPORARY STORAGE
; R6-N
; R7-START ADDRESS OF ARRAY
;-----
; Q_RCR7J ; ARRAY START ADDRESS-Q
;-----

START: ALU_LA-KC.1J,
LA_RACR3J ; K-1 TO K
;-----
RCR3J_ALU ;
;-----
RCR1J_ALU,
ALU_KC.1J ; I=1
;-----
LOOP: D_LA,
LA_RACR3J ; K--D
;-----
ALU_D-LB,
LAB_RCR1J,CLK,UBCC ;K-I IN ALU
;-----
ALU_N? ; K>I?
;-----
=0111 ;K>I
D_ALU.LEFT2,
ALU_RCR1J ; I*4 TO D
VA_ALU,
ALU_QC+1D,J/PP ;GET ARRAY(I) ADDRESS
;-----
; K<I
ALU_LA-KC.6J,
LA_RACR3J,CLK,UBCC;K-0
;-----
C31? ; K>0?
;-----
=0 ; C31=0 K>0
J/START ; BACK TO START
;-----
; C31=1 K<=0
PC_PC+1,CLR.IB.OPC,J/062 ; STOP
;-----
PP: DCLONGJ_CACHE ; READ FROM MEMORY
;-----
RCR4J_DJ
;-----
LAB_RCR4J ; ARRAY(I) TO LA
;-----
VA_VA+4,LAB_RCR4J; GET ARRAY(I+1) ADDR
;-----
DCLONGJ_CACHE ; READ ARRAY(I+1) TO D
;-----
ALU_LA-D,CLK,UBCC ; ARRAY(I)-ARRAY(I+1)
;-----
LAB_RCR1J,ALU_N? ; I TO LB
;-----
=0111 ;ALU.N=0,ARRAY(I)>ARRAY(I+1)
;-----
;ALU.N=1,ARRAY(I+1)<=ARRAY(I)
VA_ALU,
ALU_Q+LB ;ARRAY(I+1) ADDRESS TO VA
;-----
CACHE_DCLONGJ,
ALU_Q+LB-1 ;WRITE (ARRAY(I)) TO ARRAY(I+1)
;-----
VA_ALU ;ARRAY(I) ADDRESS TO VA
;-----
D_RCR4J ;ARRAY(I+1) TO D
;-----
CACHE_DCLONGJ,
J/LOOP ;WRITE (ARRAY(I+1)) TO ARRAY(I)
;-----
;END BUBBLE SORT

```

Figure 3- Microcode Source
Program for MICRO 2 Assembler

Initially a source file name followed by ,MIC is entered which notifies the VAX/VMS operating system that the editor is creating source microcode modules. By using the command \$MICRO 2, "file name", the operating system is notified that the MICRO 2 assembler is to be used to create a microcode load module which will be identified as ,MCR and will be file ,MCR; N where N is the number of Micro Assemblies executed. The MICRO 2 language lets the microprogrammers express the actions

of a microprogram symbolically. The MICRO 2 assembler translates this symbolic representation into micro control words. MICRO 2 also allocates control storage space to any microwords for which it isn't specifically identified. In allocating control storage address, the microprogrammer has three choices:

- Allocating control storage location for a microword absolutely.
- Specifying a constraint on its control storage allocation of a microword e.g. making the lowest order bits of the address equal zero.
- Letting MICRO 2 determine the microword allocation.

MICRO 2 detects syntax errors in the source microprogram. The syntax checking is based on two parts:

- First, it checks whether the statements are recognizable by MICRO 2. Unrecognizable statements create an error message.
- Second, a check of data path conflicts is made. If the data paths overlap for a particular microinstruction, an error message is generated.

The MICRO 2 source language also contains some "pseudo-operations" which don't generate microcode but give commands to the assembler. This is done by either specifying a command to the assembler, or by influencing the output of the assembler. In order to simplify the writing of a microprogram, the VAX 11/780 "user" microprogram support offers a group of MACRO definitions expressed in a language recognized by MICRO 2. These MACRO definitions are presented in the VAX 11/780 microprogramming tools user's guide.

They are categorized as described below:

.ALU_0 . . . thru ALU_D.AND . . .
.ALU_D(8). . thru ALU_D.XOR

```

;ALU_K . . . thru ALU_PC . . .
;ALU_Q . . . thru CACHE_ . . .
;D_O . . . thru D_CACHE
;D_DAL . . . thru D_D . . .
;D_INT.SUM . . .thru D_PC . . .
;D_Q . . .
;D_R . . . thru D & VA_ . . .
;EALU_ . . . thru FE_ . . .
;ID_ . . . thru LC_ . . .
;PC_ . . . thru PC & VA_ . . .
;Q_O . . . thru Q_D . . .
;Q_IB . . . thru Q_PC
;Q_Q . . . thru Q & VA_ . . .
;R[ ]_O . . . thru R[ ]_PACK.FP
;RC[ ]_O . . . thru RC [ ]_D . . .
;SC_O(A)
;SD_ . . . thru VA_ . . .
;MATCH States
;Non transfer functions
;Branch enable Macro definitions

```

If the microprogrammer doesn't find a MACRO which satisfies a requirement, two steps can be taken. One is to specify the data path and microoperations directly which is time consuming and difficult. The second is to define a new Macro which accomplishes the desired CPU action.

3) How to load and execute a microprogram.

Upon completion of the generation of a source microprogram in the MICRO 2 assembly language including corrections to all errors detected, the next step is to load the microprogram into "user" control storage. This is accomplished by first assembling the source microprogram by issuing the command:

\$MICRO 2 file name and depressing the return key.

The MICRO 2 assembler assembles the source program and produces a listing file (.MCR). To obtain a copy of the assembled program, issue the command:

\$TYPE or PRINT file name .MCR and depress the return key.

Depending on the type of terminal being used the response will be a listing either on the CRT display, a keyboard printer (TYPE) or on a line printer (PRINT). The listing shows the source program and the corresponding microcode. It also indicates syntax errors if any exist. When all errors are corrected, use the command:

\$MICLD

The assembled program is loaded into writable control storage (WCS). The accomplishment of this load is specified at a CRT terminal by the appearance of the prompt symbol indicating that the VMS control program is awaiting the next command. In order to execute the assembled microprogram it is necessary to transfer control of the VAX 11/780 CPU over to the microcode now resident in the WCS. This requires a command to the Virtual Machine System (VMS). To do this an invoking program written in VAX MACRO assembler language is required. The VAX 11/780 MACRO assembly language has an extended function call, (XFC), instruction which transfers control from VMS to the microcode in WCS. The invoking program must also set up any parameters to be passed to the microcode either by inserting values in registers or through a parameter list in main memory. A pointer to this parameter list must be stored in a register. Also to be able to check the result of running a microprogram a labeled NOP instruction serves as a breakpoint which can be used to check the result of executing microcode by using the MACRO Debug facility. The sample invoking program which in addition to executing the microcode in WCS also measures microcode execution time is shown in figure D5.

```

TYPE SORTTEST.MAR
.TITLE          SORTTEST
.ENTRY          SORTTEST, "H<"
$CHKRNLS        ROUTIN=SAVEC      ;SAVE AND CHANGE XFC VECTOR IN SCB.
$CREATE         FAB=OUTFAB
$CONNECT        RAB=OUTRAB
$ASCTIM_S       ,TIMBUF=ATIMENOW,,
MOV3            #32,ATIMENOW,TIMOUT
$PUT            RAB=OUTRAB-
MOVAL           AR,RO      ;STARTING ADDR OF ARRAY
;-----
XFC
;-----
$CHKRNLS        ROUTIN=RSVEC
$EXIT_S
$ASCTIM_S       ,TIMBUF=ATIMENOW,,
MOV3            #32,ATIMENOW,TIMOUT
$PUT            RAB=OUTRAB
$CLOSE         FAB=OUTFAB
;-----
SAVEC:          .WORD      0
MOVL            SCB$AL_BASE+20,RIVEC
MOVL            #2,SCB$AL_BASE+20
RET
;-----
RSVEC:          .WORD      0
MOVL            RIVEC,SCB$AL_BASE+20
RET
;-----
RIVEC:          .PSECT    VECTOR, LONG
                .LONG      0
                .LONG      0
;-----
OUTFAB:         $FAB      FNM=TIMBF,RFM=FIX,MRS=TIMSIZ,RAT=CR
OUTRAB:         $RAB      FAB=OUTFAB,RBF=TIMOUT,RSZ=TIMSIZ
TIMOUT:         .BLKB     32
                TIMSIZ=-TIMOUT
ATIMENOW:       .LONG     20%-10%
                .LONG     10%
10%:           .BLKB     32
20%:           .BLKB     0
AR:             .BLKL     255
                .END      SORTTEST
$

```

Figure 5 Microcode Invoking Program in VAX 11/780
MACRO Language

The steps to use the VMS commands to execute the MACRO invoking program assuming the microprogram is loaded in WCS are:

\$ MACRO invoking file name

\$ LINK invoking file name + SYS \$ System:SYS.STB/SEL

\$ RUN invoking file name

Execution begins under VMS of the MACRO invoking program and when the XFC instruction is encountered, the microcode is executed. Control is returned to VMS and the balance of the assembly language program is executed.

4) Control Command to Debug the "User" Microprogram.

It is Very important to have a debug facility to check the MICRO Code when it is running in WCS. MICRO 2 includes commands that can cause the microprogram to be executed step by step or to execute up to any microinstruction in the microprograms in WCS. A list of user's commands and terminal reaction is shown below:

USER	COMMAND	TERMINAL INFORMATION	COMMENTS
Prompt	Command		
\$	MACRO File Name	Nothing, if nothing is wrong	Assemble the invoking program
\$	LINK File Name SYSTEM:SYS. STB/SEL	Nothing, if nothing is wrong	Link the invoking program
\$	MICRO 2 File Name	Nothing, if nothing is wrong	Assemble the microcode
\$	MICLD File Name	WCS Load Complete	Loads microcode into WCS
\$	CTRL	Show >>>	Turn to microprogram
\$	RUN File Name	>>> WCS	Start Execution of invoking Program & invokes WCS Debugger
>>>	SE SOMM	Show >>>	Set-Stop on Micro Match SOMM
>>>	H	Halted at XXX	Halt
>>>	C	Nothing	Continue
WCS >	C	Message as appropriate when execution stops	Continue to execute next instruction
WCS >	E RA []	Show content of register RA (HEX)	Exam the content of RA []
WCS >	E DR	Show content of D register	
WCS >	RET	>>> Information on CPU status	Return to MACRO Control
>>>	Show	Shows CPU status	
>>>	E/ID 21	E: Examine ID: Internal Register 21: SOMM Register	

APPENDIX C

QUADRUPLER DEFINITIONS

The following quadruplet definitions are to be considered standard for the interface between the PASCAL and XPL to quadruplet compilers and the Quadruplet to VAX MACRO (Assembly Language) and MICRO 2 (Microcode) translators.

Two formats are described below. One is for the complete quadruplet while the second is for operands 1, 2 and 3:

Quadruplet Format:	Operation	Data Type	Operand 1	Operand 2	Operand 3
	<u>14</u> <u>17</u>	22	<u>25</u> <u>35</u>	<u>38</u> <u>48</u>	<u>51</u> <u>61</u>
	XXXXXXXX	I R b			

Operand Format

Operand 1	25	26	27	35
Operand 2	38	39	40	48
Operand 3	51	52	53	61
	#	U	N	N
	@	T		
		N		

R
I

@
\$
T
U
N

Operands are real values
Operands are integer values
Operand is a numeric value
Operand is an address of a data item

Operand is temporary location in storage on a register
Operand is a storage address assigned to a data item
Numeric value

OPERATOR	OPRND 1	OPRND 2	OPRND 3	FUNCTIONAL DEFINITION
MOV	# N UNNNNNNNNN T @		UNNNNNNNNN T @	Move numeric, storage location, Temporary storage location or indirect address value specified in operand 1 to the storage or temporary storage location or as an indirect address in operand 3.
ADD/SUB	# N UNNNNNNNNN T		UNNNNNNNNN T	Add/Sub, storage location, or temporary storage location value to/from the numeric, storage location, or temporary storage location value specified in operand 1 and place the storage or temporary storage location of the result and value in operand 3.
ADD/SUB	# N UNNNNNNNNN T	# N UNNNNNNNNN T	UNNNNNNNNN T	Add/Sub numeric, storage location, or temporary storage location value specified in operand 2 to/from numeric, storage location or temporary storage location value specified by operand 1 and place the storage or temporary storage location of the resultant value in operand 3.
SHLA/SHRA	UNNNNNNNNN T	# N UNNNNNNNNN	UNNNNNNNNN T	Shift storage location or temporary storage location value specified in Operand 1 by an amount specified by the numeric value specified in operand 2 and place the shifted resultant value in the storage or temporary storage location specified in operand 3.

OPERATOR	OPRND 1	OPRND 2	OPRND 3	FUNCTIONAL DEFINITION
INDX	UNNNNNNNNN T	UNNNNNNNNN T	UNNNNNNNNN T	Add the storage or temporary storage value specified in operand 2 to the storage or temporary storage value specified in operand 1 and place the resultant and value in the storage or temporary storage location specified by operand 3.
LT/GT/ET	# N UNNNNNNNNN T	# N UNNNNNNNNN T	TNNNNNNNNNN	Subtract the numeric, storage or temporary storage location value specified in operand 2 from the numeric, storage or temporary storage location value specified in operand 1 and check the sign and zero output flags. For LT and sign + store 1 for True in temporary storage location specified by Oprnd 3. For GT and sign - store 1 for true in temporary storage location specified by Oprnd 3. For ET and zero flag set store 1 for true in temporary storage location specified by Oprnd 3.
BRT/BRF	NNNNNNNNNN	UNNNNNNNNN T		Branch to the storage address specified in operand 1 which is either a label or an absolute address if the value stored in the storage or temporary storage location specified in operand 2 is 1 for true (T) or 0 for False (F).
BR	TNNNNNNNNNN U			Branch to the storage address specified in operand 1

OPERATOR	OPRND 1	OPRND 2	OPRND 3	FUNCTIONAL DEFINITION
BE/BG/BL	NNNNNNNNNN	UNNNNNNNNN T	UNNNNNNNNN T	Branch to the storage address specified in operand one if the result of subtracting the storage or temporary storage location value specified in operand 3 from the storage or temporary storage location value specified in operand 2 is = 0 (E); > 0 (G); < 0 (L);
Byte/Half/Full		NNNNNNNNNN		The number of bytes/half words/full words/ of storage space to be allocated to a variable specified in a immediately preceding ADDR quadruple is specified by the numeric value in operand 2.
ADDR	UNNNNNNNNN		NNNNNNNNNN	The storage location is specified in operand 1 and the quadruple number of the corresponding Byte/Half/Full quadruple is specified by operand 3.
END				Indicates end of quadruples for a procedure
RET				Indicate a return to a calling procedure
UNST				Indicates that certain variables associated with this procedure should be removed from the compiler stacks.

APPENDIX - D
QUADRUPLES TO MICRO CODE SPECIFICATION

ASSUMPTIONS:

- 1) The constant which does not exist in Fk, Sk would be stored in Reg C
- 2) ① Micro Routine if constant is in Sk
 ② Micro Routine if constant is not in Sk
- 3) #-Numerical Value
- 4) S - Storage Address
- 5) T - Temporary Storage Address
- 6) S(R) - Storage Address in Register
- 7) RA [] - A Register value
 RB [] - B Register value
 RC [] - C Register value
- 8) D [] - D Register value
 Q [] - Q Register value
- 9) @R - Indirect address of variable in storage stored in a register
 @T - Indirect address of variable in storage stored in a temporary storage location
- 10) ADDR - Branch Address

QUAD OPERATOR	QUAD OPERAND	MICRO 2
MOV	#, ,S(R.)	<p>① R[x]_K[#]; If the const exist in K</p> <p>② LC_RC[]; If the const did not exist in K R[RX]_LC;</p>
MOV	#, ,S	<p>① D_K[#]; VA_RC[]; Cache_D[];</p> <p>② D_RC[]; VA_RC[]; Cache_D[];</p>
MOV	S, ,S(R)	<p>VA_RC[]; D[]_Cache; R[]_D;</p>
MOV	S, ,S	<p>VA_RC[]; D[]_Cache; VA_RC[]; Cache_D[];</p>
MOV	@T ₁ , ,@T ₂	<p>VA_R[T₁]; D[]_Cache; VA_R[T₂]; Cache_D[];</p>
MOV	@T, ,S	<p>VA_R[T]; D[]_Cache; VA_R[T₂]; Cache_D[];</p>
MOV	#, ,@T	<p>① D[]_K[#]; VA_R[]; Cache_D[];</p> <p>② D[]_RC[]; VA_R[]; Cache_D[];</p>
INDX	R, # ,T	<p>① LAB_R[R]; ALU_LA + K[#], R[]_ALU;</p> <p>② D_RC[]; ALU_D + K[#], R[]_ALU;</p>
GT	S, # ,T	<p>① Q_K[#]; ALU_LA_Q, LAB_R[], CLK.UBCC; ALU ? ;</p>

=1110

J/ADDR;

QUAD OPERATOR	QUAD OPERAND	MICRO 2
		② Q_RC[]; ALU_LA_Q, LAB_R[], CLK_UBCC; ALU ? ; = 1110 J/ADDR;
GT BRT	S ₁ , S ₂ , T ADDR, ,	Q_R[S ₂]; ALU_LA_Q, LAB_R[S ₁], CLK_UBCC; ALU ? ; = 1110 J/ADDR;
ADD	# , S(R), S(R)	① LAB_R[S], ALU_LA + K[], R[S]_ALU; ② Q_RC[]; LAB_R[S]; ALU_LA + Q, R[S]_ALU;
ADD	S ₁ (R), S ₂ (R), S ₃	VA_RC[], LAB_R[S ₁]; { LA_R[S ₂], ALU_LA[+]LB, D_ALU; Cache_D[Long];
SUB	S(R), # , S(R)	① LAB_R[S]; ALU_LA_K[]; R[S]_ALU; ② Q_RC[]; LAB_R[S]; ALU_LA_Q, R[S]_ALU;
SUB	S ₁ (R), S ₂ (R), S ₃	VA_RC[], LAB_R[S ₂]; { LA_R[S ₁], ALU_LA[-]LB, D_ALU; Cache_D[Long];
END	, ,	PC_PC + 1, CLR_IB.OPC, J/062;

